EE 330
Lecture 37

Digital Circuit Design

- Characterization of CMOS Inverter
- One device sizing strategy

Exam Schedule

Exam 1	Friday Sept 24
Exam 2	Friday Oct 22
Exam 3	Friday Nov 19
Final	Tues Dec 14 12:00 p.m.

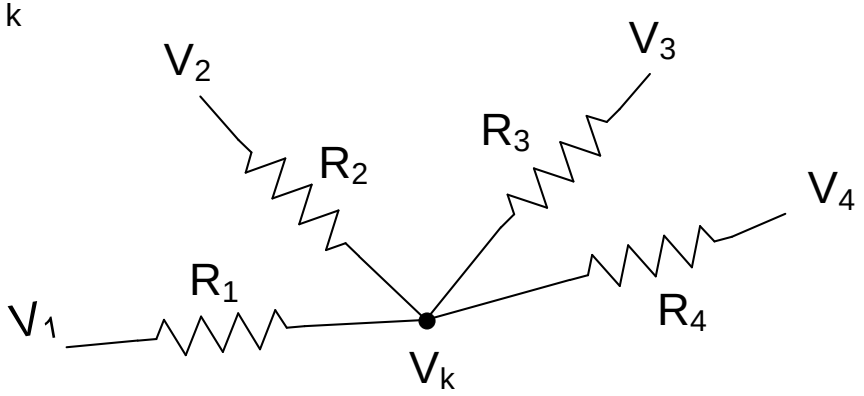
As a courtesy to fellow classmates, TAs, and the instructor

Wearing of masks during lectures and in the laboratories for this course would be appreciated irrespective of vaccination status

Nodal Analysis (A Brief Review)

Widely used to analyze electronic circuits – and for good reason!

Example: Determine V_k



From KCL

$$\left(\frac{V_k - V_1}{R_1}\right) + \left(\frac{V_k - V_2}{R_2}\right) + \left(\frac{V_k - V_3}{R_3}\right) + \left(\frac{V_k - V_4}{R_4}\right) = 0$$

$$V_k\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4}\right) = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_4}{R_4}$$

$$V_k = V_1 \frac{1}{R_1\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4}\right)} + V_2 \frac{1}{R_2\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4}\right)} + V_3 \frac{1}{R_3\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4}\right)} + V_4 \frac{1}{R_4\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4}\right)}$$

$$V_k = V_1 \frac{R_2R_3R_4}{(R_2R_3R_4 + R_1R_3R_4 + R_2R_1R_4 + R_2R_3R_1)} + V_2 \frac{R_1R_3R_4}{(R_2R_3R_4 + R_1R_3R_4 + R_2R_1R_4 + R_2R_3R_1)} + V_3 \frac{R_2R_1R_4}{(R_2R_3R_4 + R_1R_3R_4 + R_2R_1R_4 + R_2R_3R_1)} + V_4 \frac{R_2R_3R_1}{(R_2R_3R_4 + R_1R_3R_4 + R_2R_1R_4 + R_2R_3R_1)}$$

Time consuming and tedious for even simple circuits

Nodal Analysis (A Brief Review)

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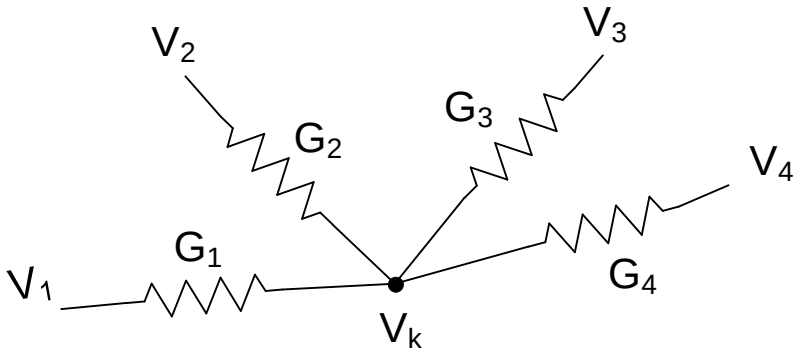


From KCL $V_k\left(G_1+G_2+G_3+G_4\right)=G_1V_1+G_2V_2+G_3V_3+G_4V_4$

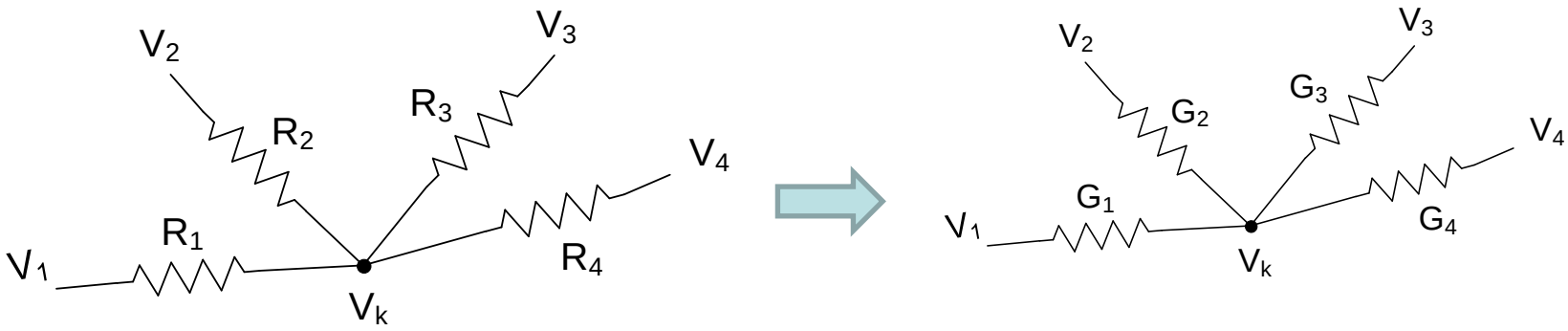
$$V_k = V_1\frac{G_1}{G_1+G_2+G_3+G_4}+V_2\frac{G_2}{G_1+G_2+G_3+G_4}+V_3\frac{G_3}{G_1+G_2+G_3+G_4}+V_4\frac{G_4}{G_1+G_2+G_3+G_4}$$

Often much simpler to work with conductances than with resistances!

And expressions much simpler

Nodal Analysis (A Brief Review)

Widely used to analyze electronic circuits – and for good reason!



And expressions much simpler (compare in standard rational fraction form)

$$V_k = V_1 \frac{R_2R_3R_4}{(R_2R_3R_4 + R_1R_3R_4 + R_2R_1R_4 + R_2R_3R_1)} + V_2 \frac{R_1R_3R_4}{(R_2R_3R_4 + R_1R_3R_4 + R_2R_1R_4 + R_2R_3R_1)} + V_3 \frac{R_2R_1R_4}{(R_2R_3R_4 + R_1R_3R_4 + R_2R_1R_4 + R_2R_3R_1)} + V_4 \frac{R_2R_3R_1}{(R_2R_3R_4 + R_1R_3R_4 + R_2R_1R_4 + R_2R_3R_1)}$$

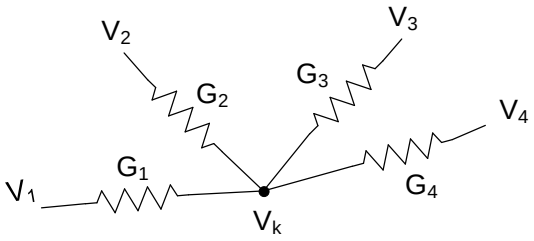
$$V_k = V_1 \frac{G_1}{G_1 + G_2 + G_3 + G_4} + V_2 \frac{G_2}{G_1 + G_2 + G_3 + G_4} + V_3 \frac{G_3}{G_1 + G_2 + G_3 + G_4} + V_4 \frac{G_4}{G_1 + G_2 + G_3 + G_4}$$

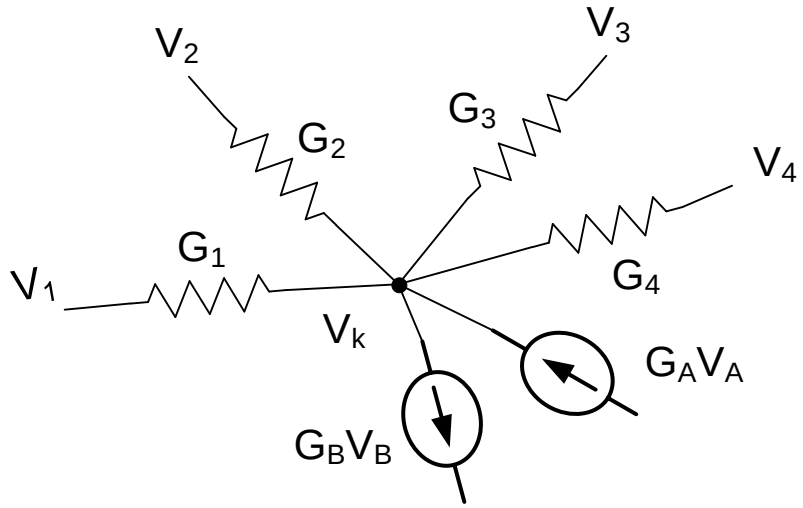
Nodal Analysis (A Brief Review)

Widely used to analyze electronic circuits – and for good reason!

Example: Determine V_k

Easy to add dependent sources





From KCL $V_k\left(G_1+G_2+G_3+G_4\right)+G_BV_B-G_AV_A=G_1V_1+G_2V_2+G_3V_3+G_4V_4$

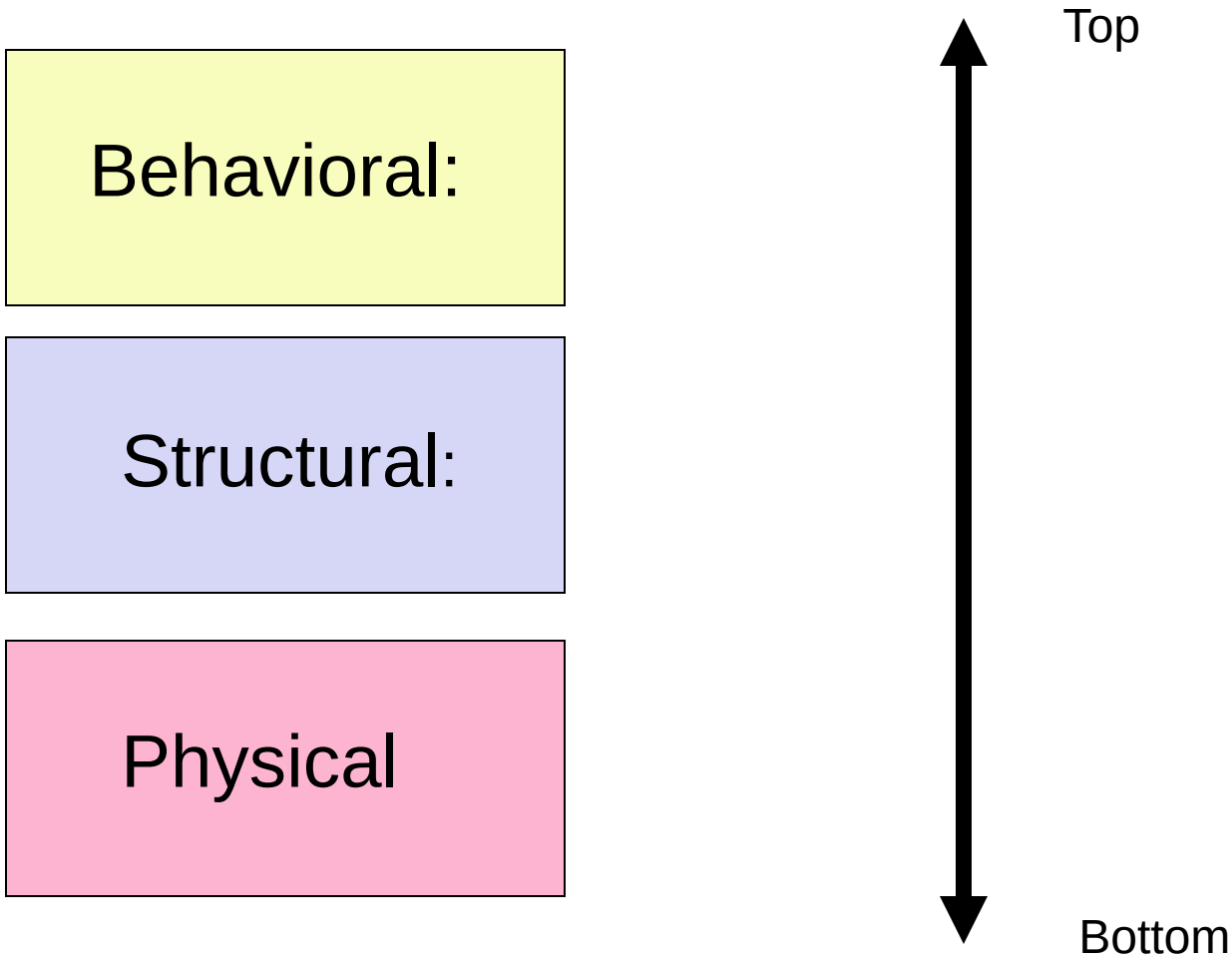
$$V_k=V_1\frac{G_1}{G_1+G_2+G_3+G_4}+V_2\frac{G_2}{G_1+G_2+G_3+G_4}+V_3\frac{G_3}{G_1+G_2+G_3+G_4}+V_4\frac{G_4}{G_1+G_2+G_3+G_4}+V_A\frac{G_A}{G_1+G_2+G_3+G_4}-V_B\frac{G_B}{G_1+G_2+G_3+G_4}$$

Often much simpler to work with conductances than with resistances!

Do we really need the concept of both a resistor and a conductor?

Review from last lecture

Hierarchical Digital Design Domains:



Multiple Levels of Abstraction

Review from last lecture

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
    - Logical Effort
  - Elmore Delay
- Sizing of Gates
  - The Reference Inverter
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

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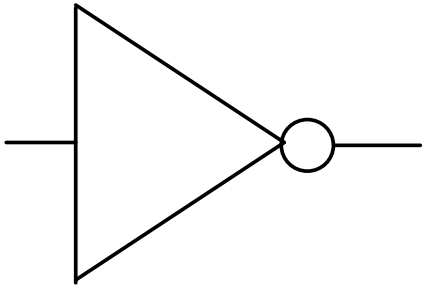
done

partial

Review from last lecture

The basic logic gates

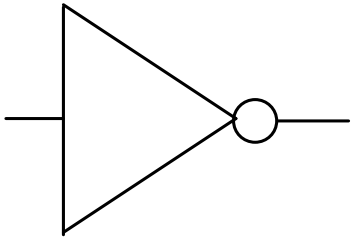
It suffices to characterize the inverter of a logic family and then express the performance of other gates in that family in terms of the performance of the inverter.



What characteristics are required and desirable for an inverter to form the basis for a useful logic family?

Review from last lecture

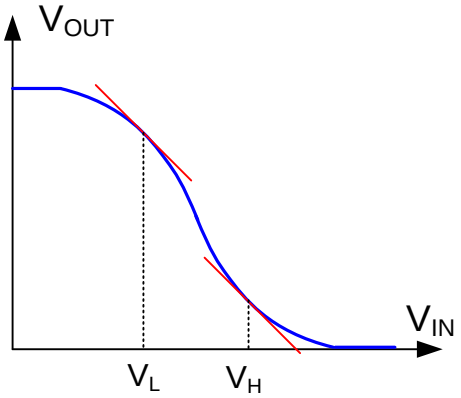
What are the logic levels for a given inverter of for a given logic family?



V_H=? V_L=?

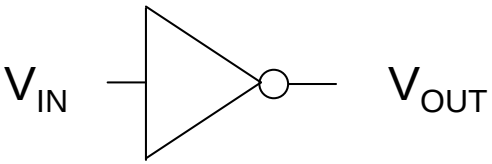
Can we legislate them ?

- Some authors choose to define them based upon specific features of inverter
- Analytical expressions may be complicated
- But what if the circuit does not interpret them the same way they are defined !!



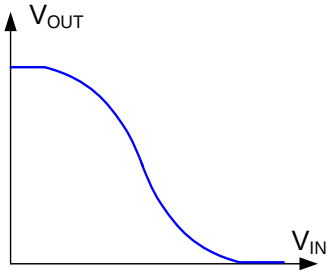
Review from last lecture

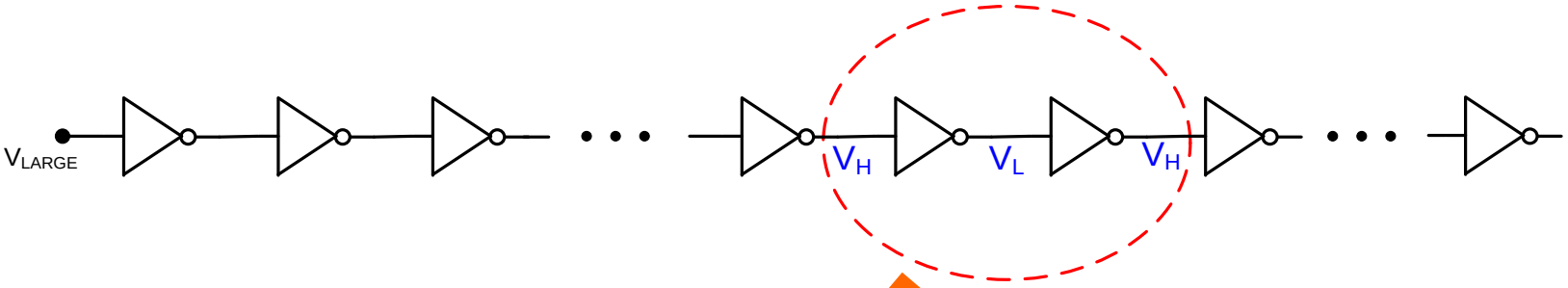
Ask the inverter how it will interpret logic levels

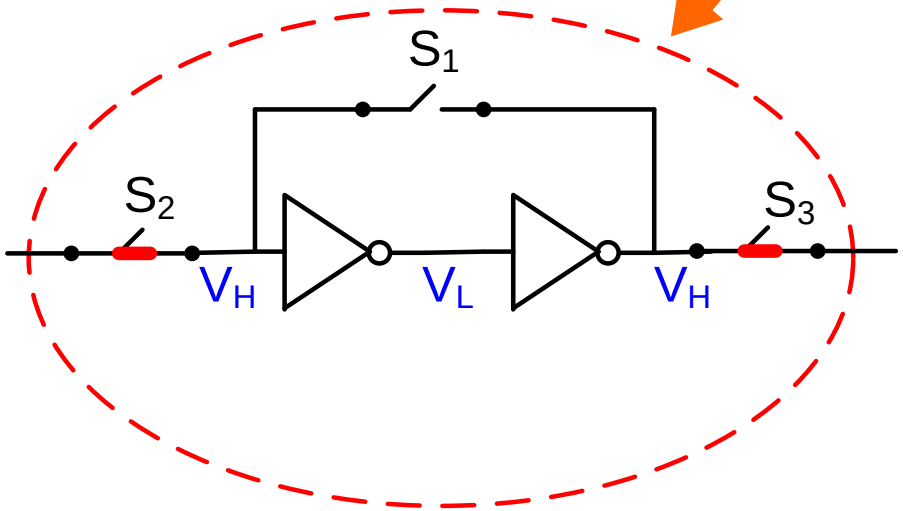


V_H=?

V_L=?

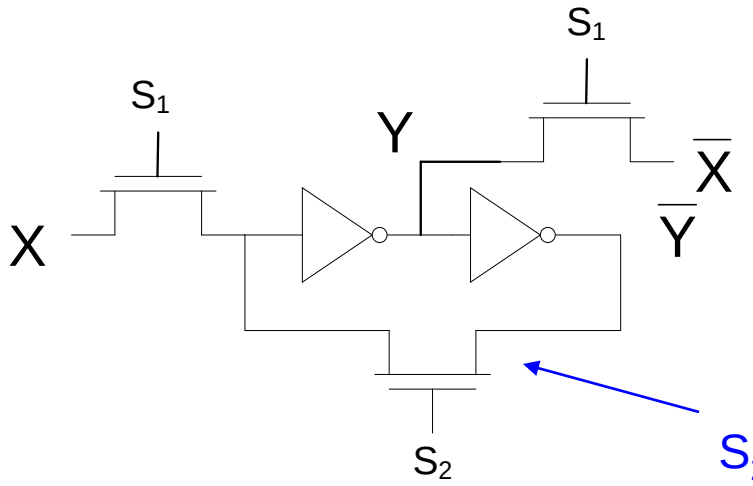




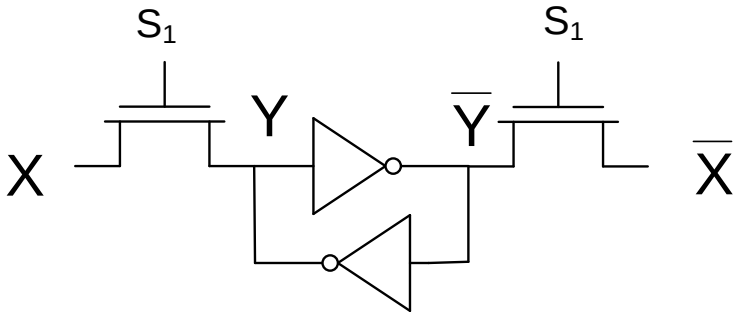


Review from last lecture

The two-inverter loop



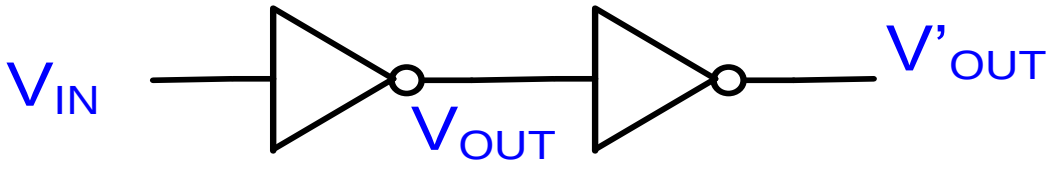
S_2 often eliminated (shorted)



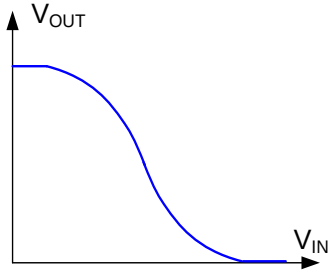
Standard 6-transistor SRAM Cell

Review from last lecture

Ask the inverter how it will interpret logic levels



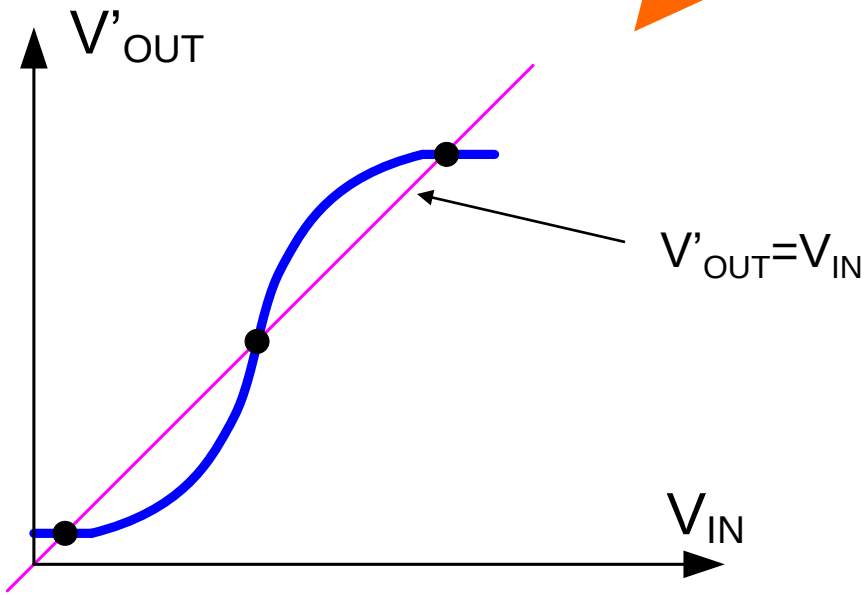
Inverter pair



V_H=?

V_L=?

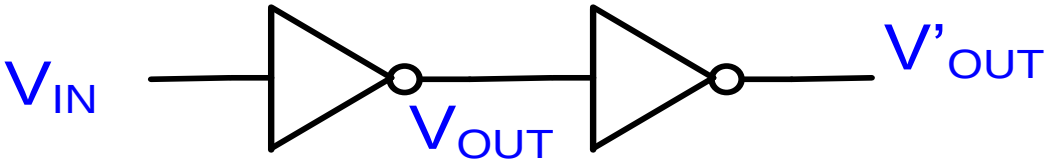
V_H and V_L will be on the intersection of the transfer characteristics of the inverter pair (IPTC) and the $V'_{OUT}=V_{IN}$ line



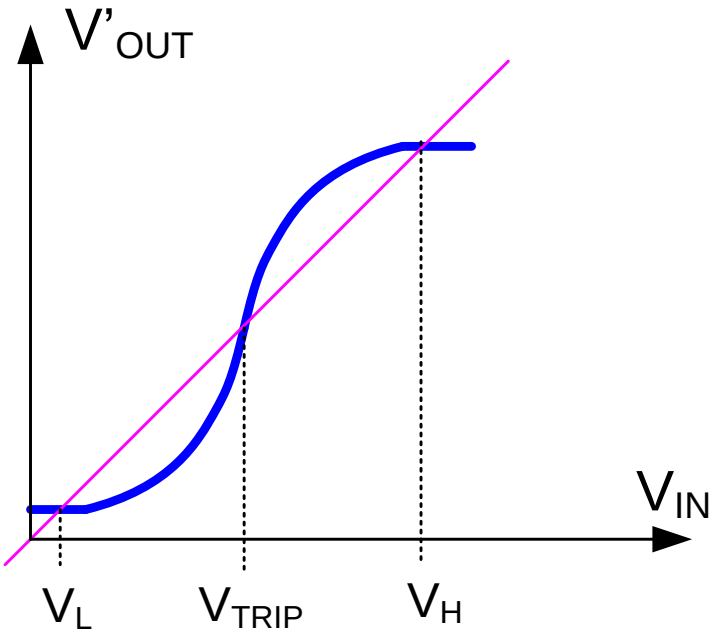
V_H and V_L often termed the “1” and “0” states

Review from last lecture

Ask the inverter how it will interpret logic levels



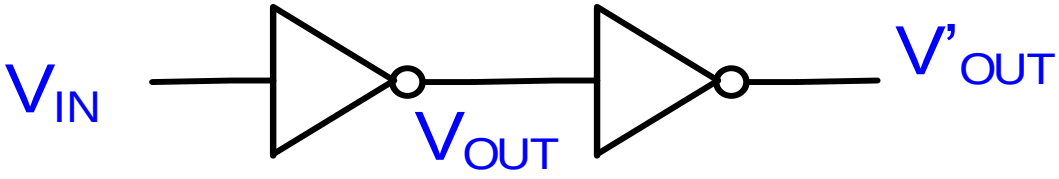
Inverter pair



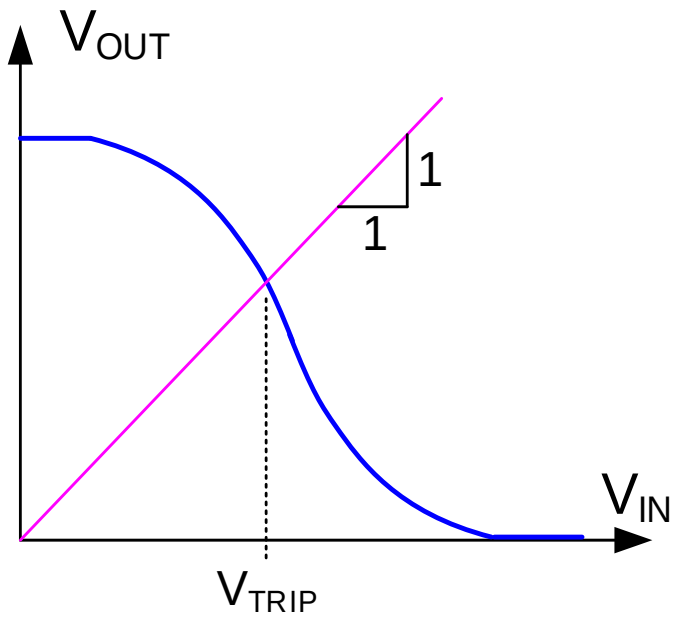
When $V'_{OUT}=V_{IN}$, V_H and V_L are stable operating points, V_{TRIP} is a quasi-stable operating point

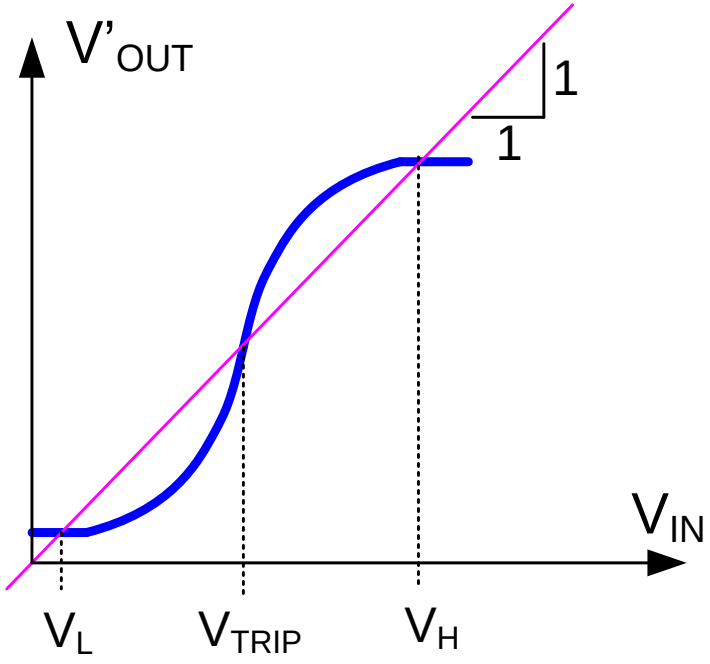
Observe: slope of IPTC is greater than 1 at V_{TRIP} and less than 1 at V_H and V_L

Observation



When $V_{OUT}=V_{IN}$ for the inverter, V'_{OUT} is also equal to V_{IN}. Thus the intersection point for $V_{OUT}=V_{IN}$ in the inverter transfer characteristics (ITC) is also an intersection point for $V'_{OUT}=V_{IN}$ in the inverter-pair transfer characteristics (IPTC)





Implication: Inverter characteristics can be used directly to obtain V_{TRIP}

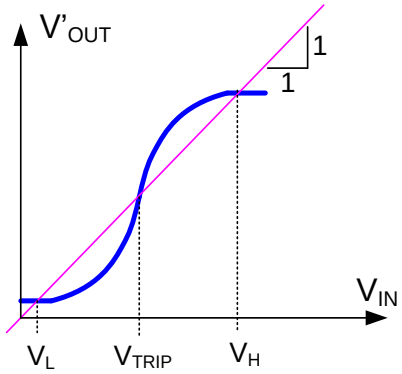
Logic Family Characteristics

What properties of an inverter are necessary for it to be useful for building a two-level logic family?

The inverter-pair transfer characteristics must have three unique intersection points with the $V'_{OUT} = V_{IN}$ line

What are the logic levels for a given inverter of for a given logic family?

The two extreme intersection points of the inverter-pair transfer characteristics with the $V'_{OUT} = V_{IN}$ line



Can we legislate V_H and V_L for a logic family ? No!

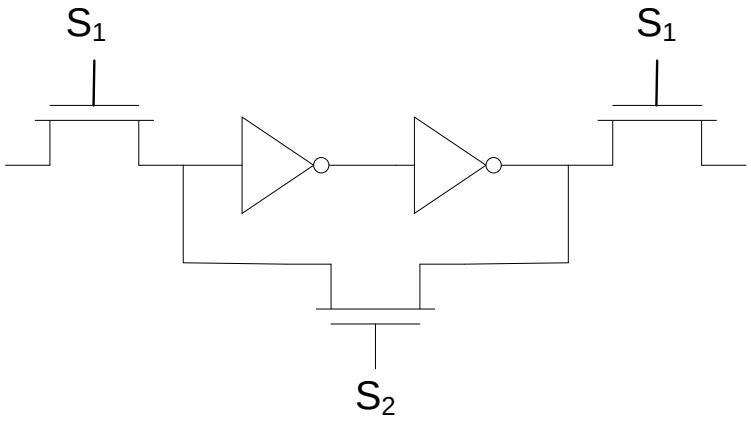
What other properties of the inverter are desirable?

Reasonable separation between V_H and V_L (enough separation so that noise does not cause circuit to interpret level incorrectly)

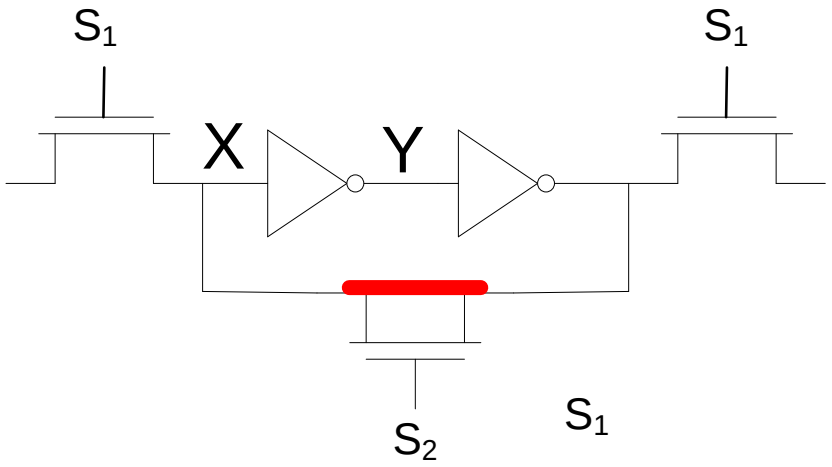
$$V_{TRIP} \cong \frac{V_H + V_L}{2}$$

(to provide adequate noise immunity and process insensitivity)

What happens near the quasi-stable operating point?

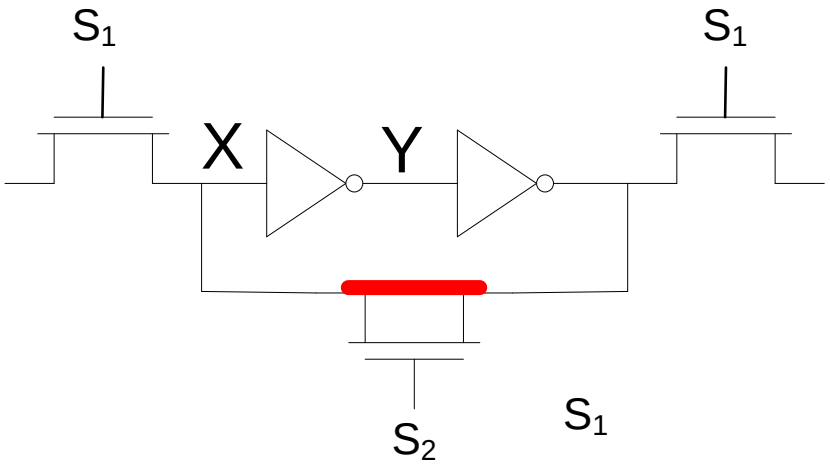


S_2 closed and $X=Y=V_{TRIP}$



What happens near the quasi-stable operating point?

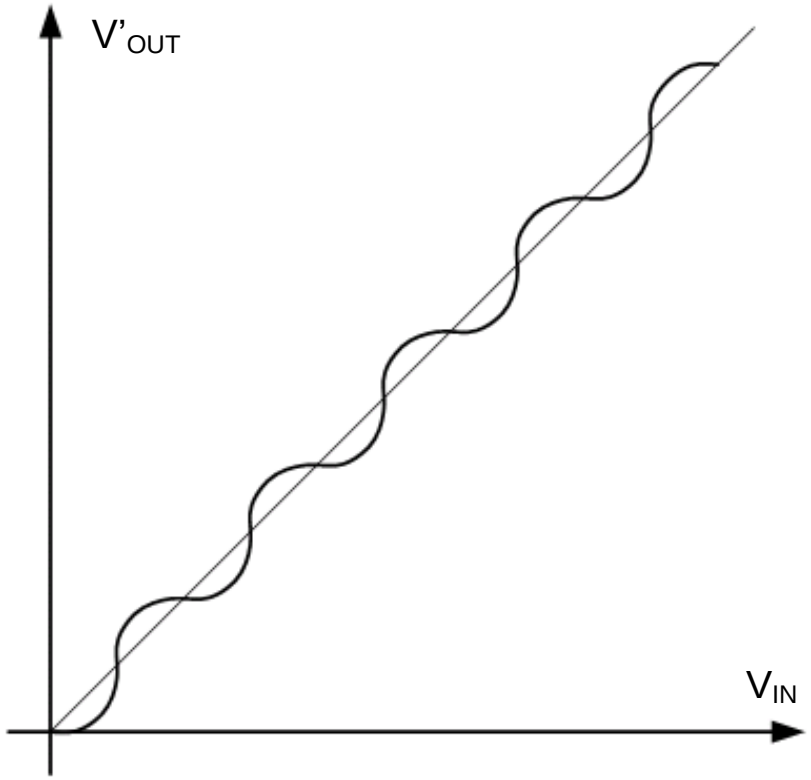
S_2 closed and $X=Y=V_{TRIP}$



If X decreases even very slightly, will move to the X=0, Y=1 state (very fast)

If X increases even very slightly, will move to the X=1, Y=0 state (very fast)

What if the inverter pair had the following transfer characteristics?



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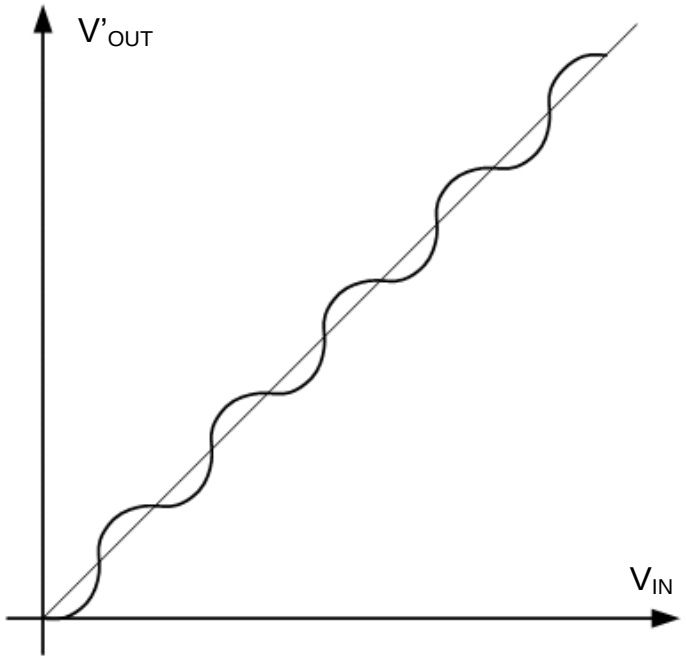
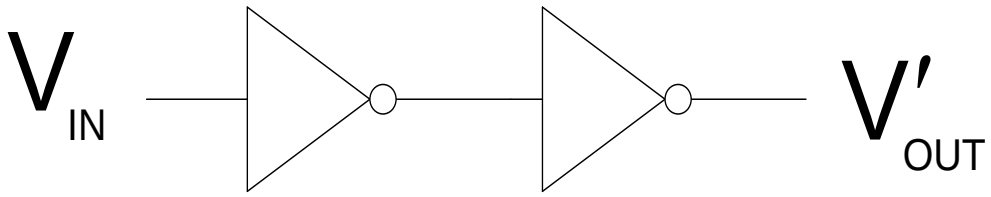
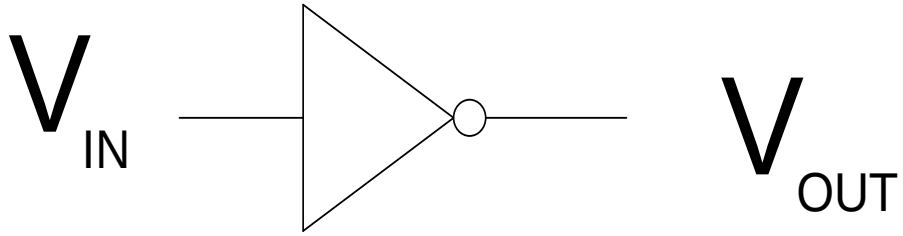


Multiple levels of logic
Every intersection point with slope <1 is a stable point
Every intersection point with slope >1 is a quasi-stable point

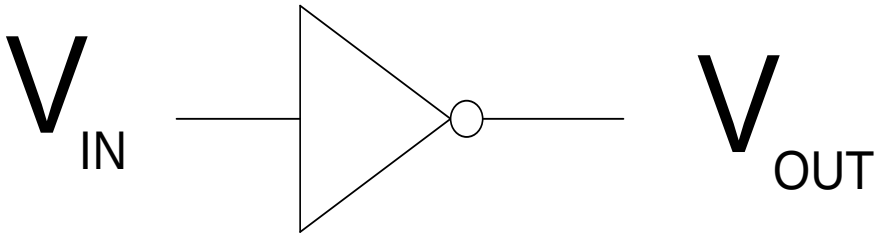
What are the transfer characteristics of the static CMOS inverter pair?

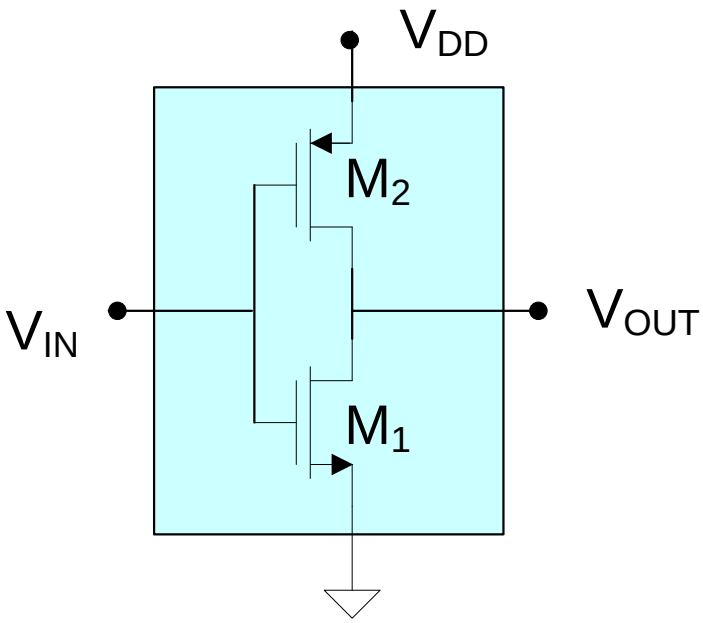


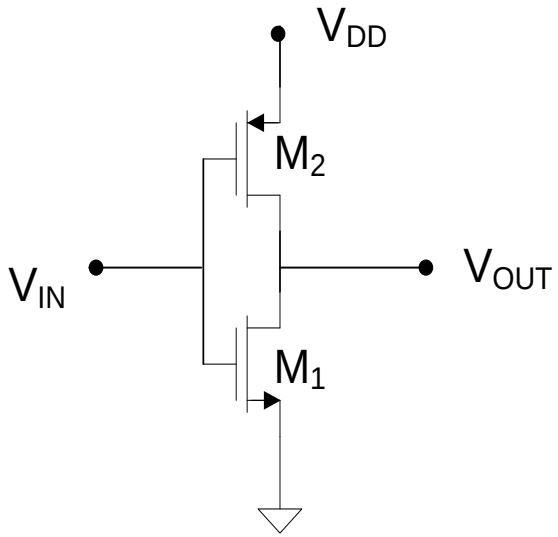
Consider first the inverter



Transfer characteristics of the static CMOS inverter






V_{DD}
M_2
V_{IN}
V_{OUT}
M_1

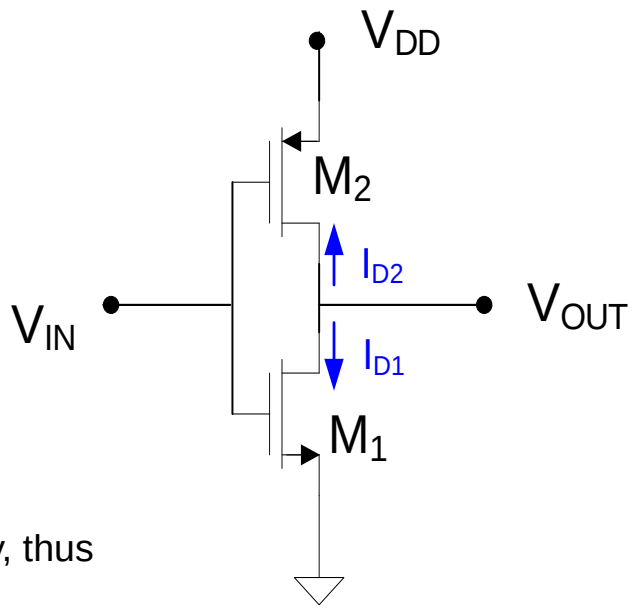
Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 1 Vin is so high that M_1 triode, M_2 cutoff

$$I_{D1} = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2}\right)V_{OUT}$$

$$I_{D2} = 0$$



Equating I_{D1} and $-I_{D2}$ we obtain:

$$0 = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2}\right)V_{OUT}$$

It can be shown that setting the first product term to 0 will not verify, thus

$$V_{OUT} = 0$$

valid for:

$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} < V_{GS1} - V_{Tn} \qquad V_{GS2} \geq V_{Tp}$$

thus, valid for:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} < V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \geq V_{Tp}$$

Graphical Interpretation of these conditions:

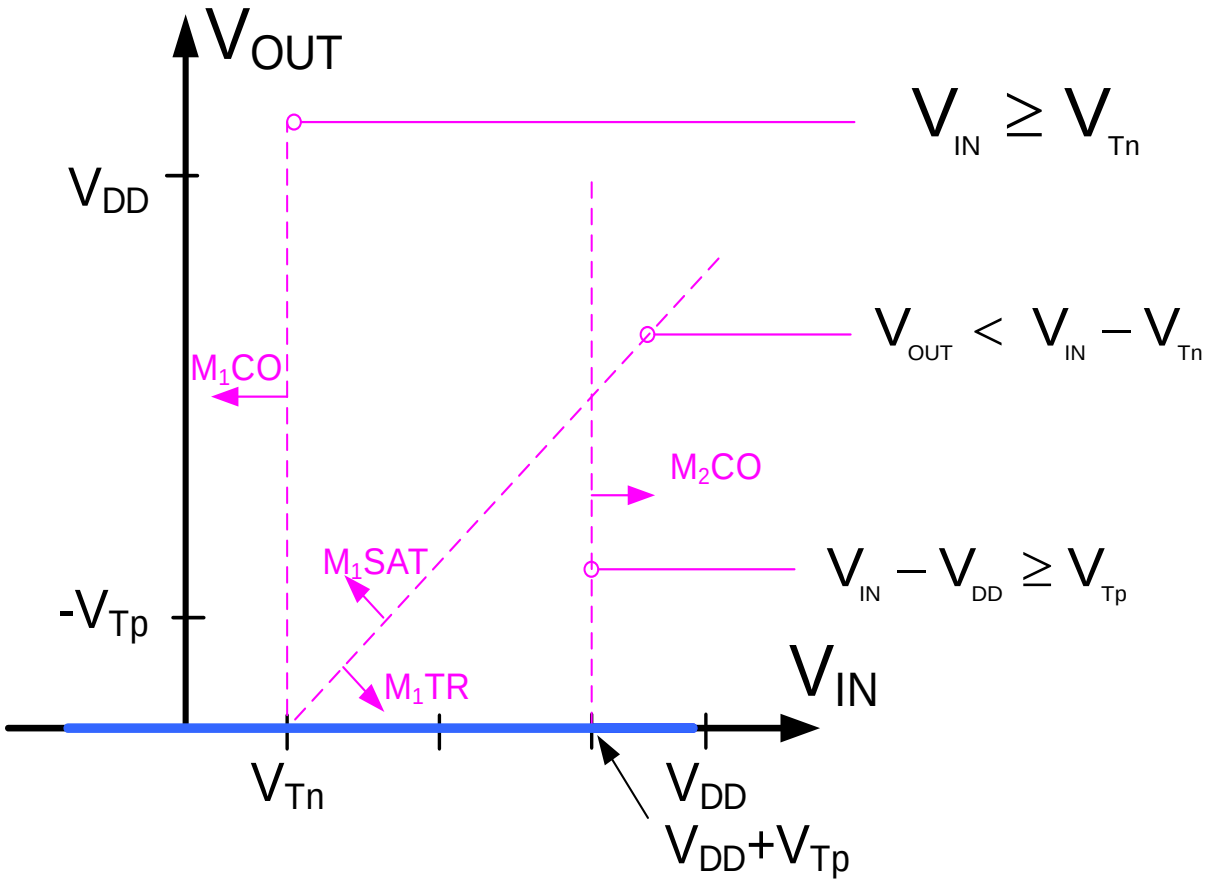
$V_{IN} \geq V_{Tn}$ $V_{OUT} < V_{IN} - V_{Tn}$ $V_{IN} - V_{DD} \geq V_{Tp}$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 1 M_1 triode, M_2 cutoff

$$V_{OUT} = 0$$

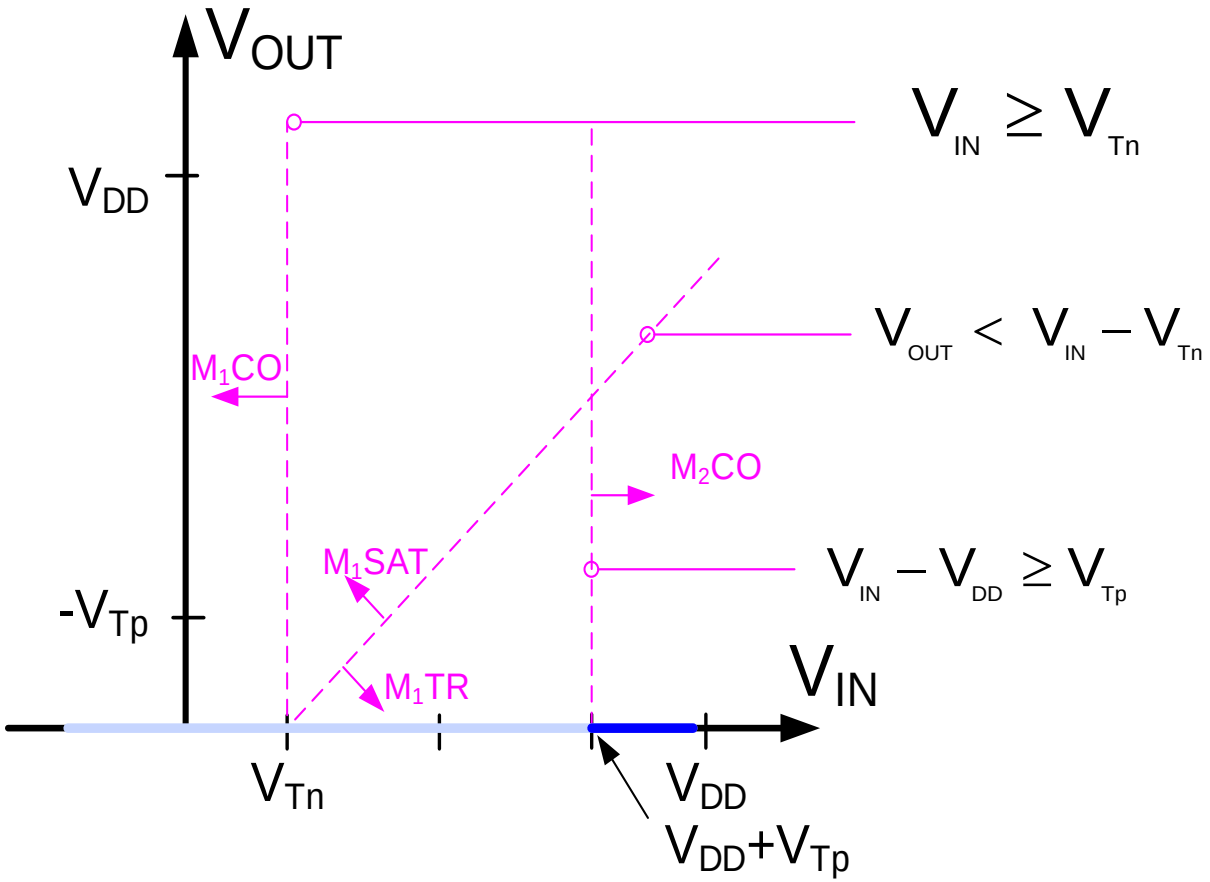


Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 1 M_1 triode, M_2 cutoff

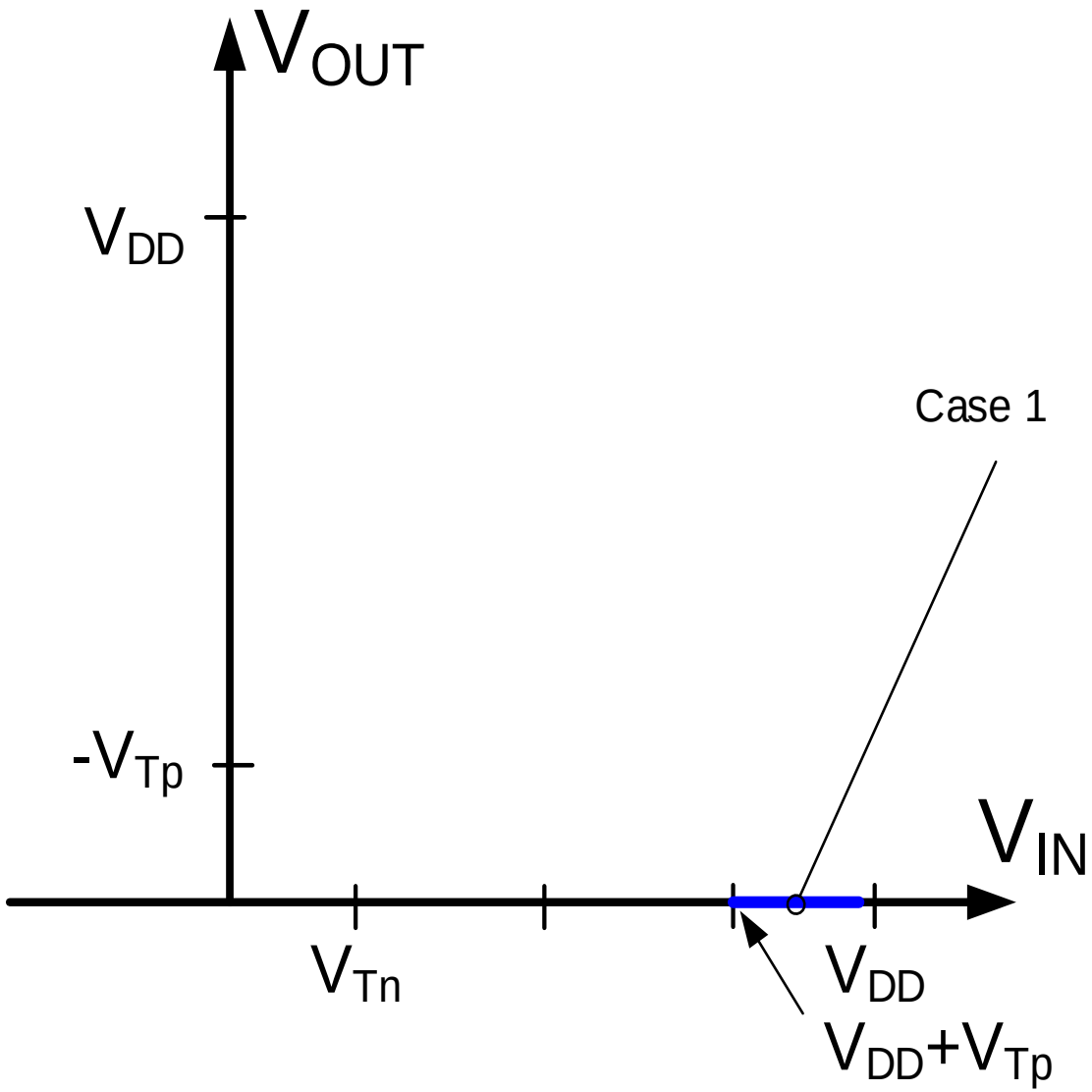
$$V_{OUT} = 0$$



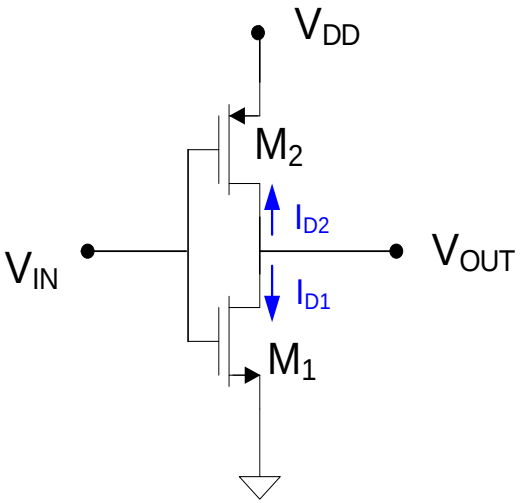
Transfer characteristics of the static CMOS inverter

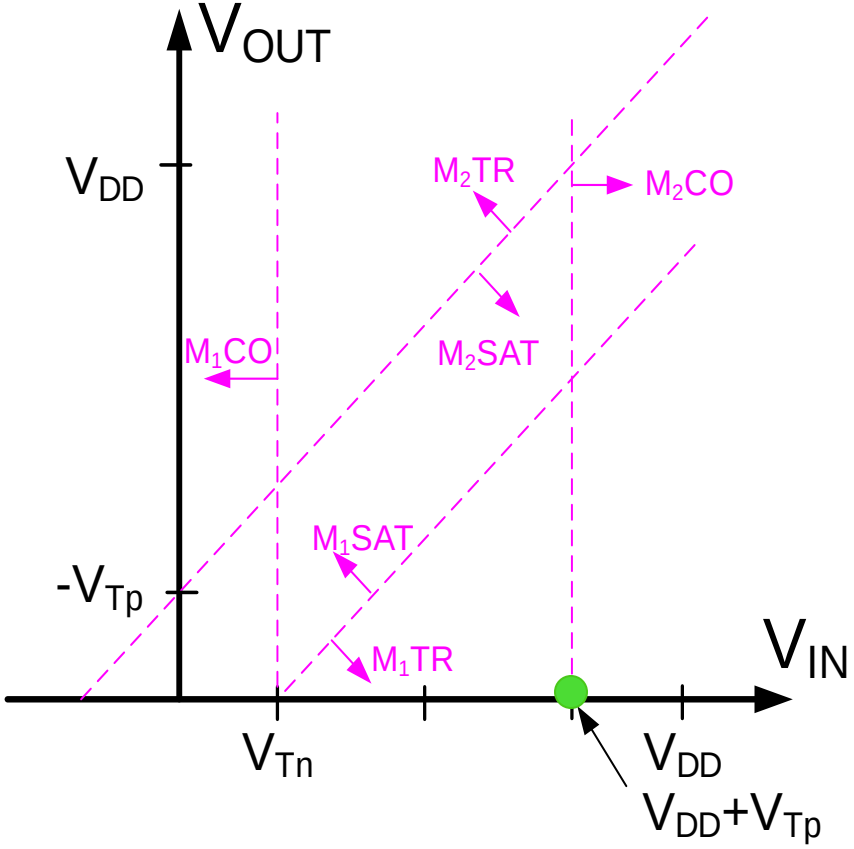
(Neglect λ effects)

Partial solution:



Regions of Operation for Devices in CMOS inverter

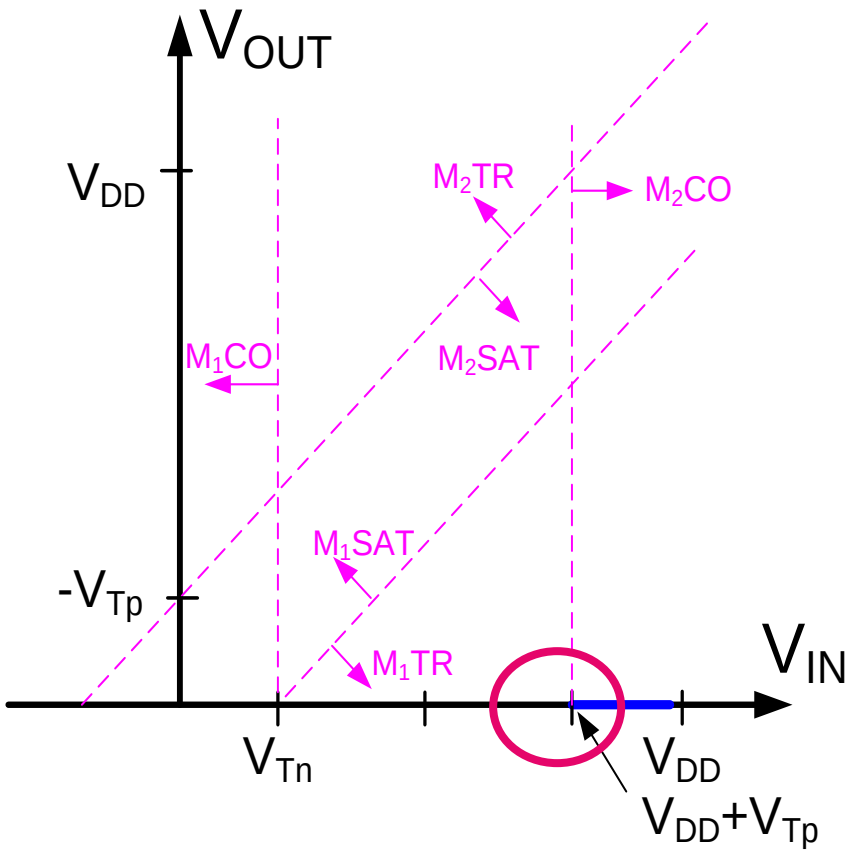




Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 2 M_1 triode, M_2 sat



M_2: Square law I_D

M_1: like a resistor

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

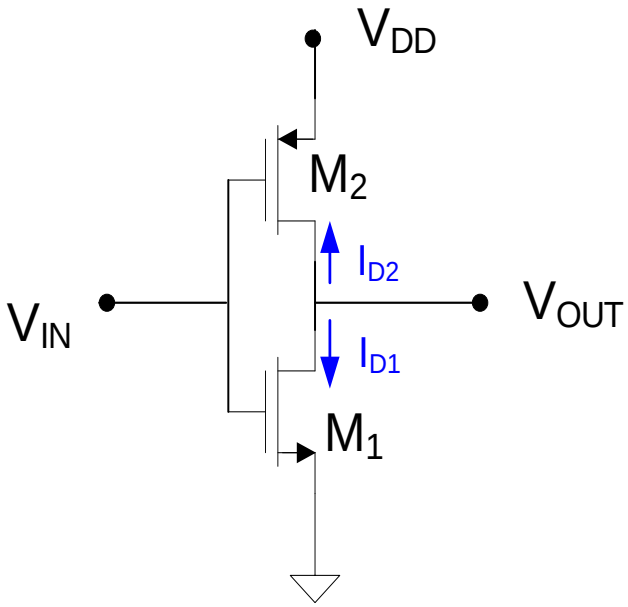
Case 2 M_1 triode, M_2 sat

$$I_{D1} = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

$$I_{D2} = -\frac{\mu_p C_{OXp}}{2} \frac{W_2}{L_2} \left(V_{IN} - V_{DD} - V_{Tp} \right)^2$$

Equating I_{D1} and $-I_{D2}$ we obtain:

$$\frac{\mu_p C_{OXp}}{2} \frac{W_2}{L_2} \left(V_{IN} - V_{DD} - V_{Tp} \right)^2 = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$



valid for:

$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} < V_{GS1} - V_{Tn} \qquad V_{GS2} \leq V_{Tp} \qquad V_{DS2} \leq V_{GS2} - V_{T2}$$

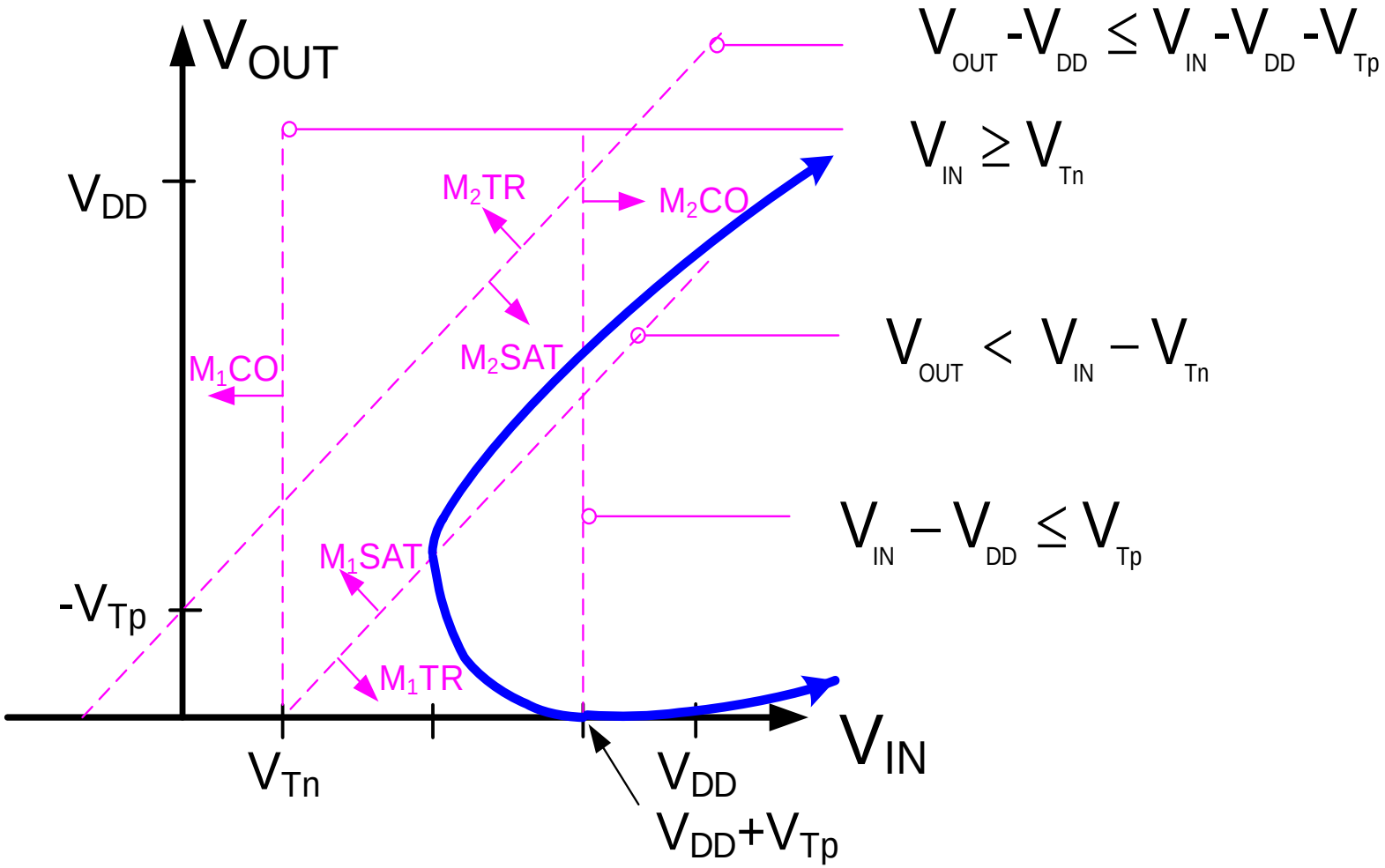
thus, valid for:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} < V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \leq V_{Tp} \qquad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

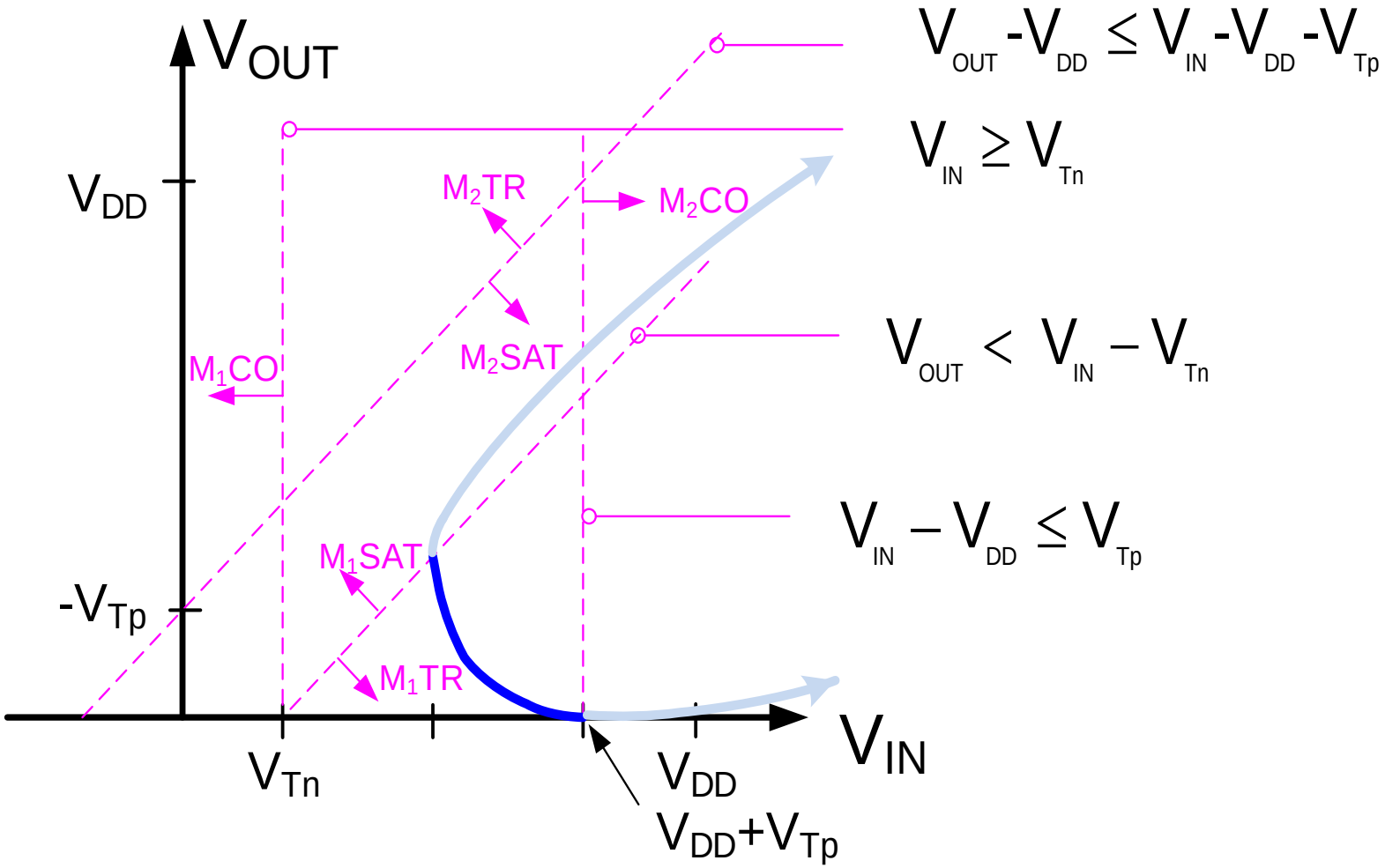
Case 2 M_1 triode, M_2 sat



Transfer characteristics of the static CMOS inverter

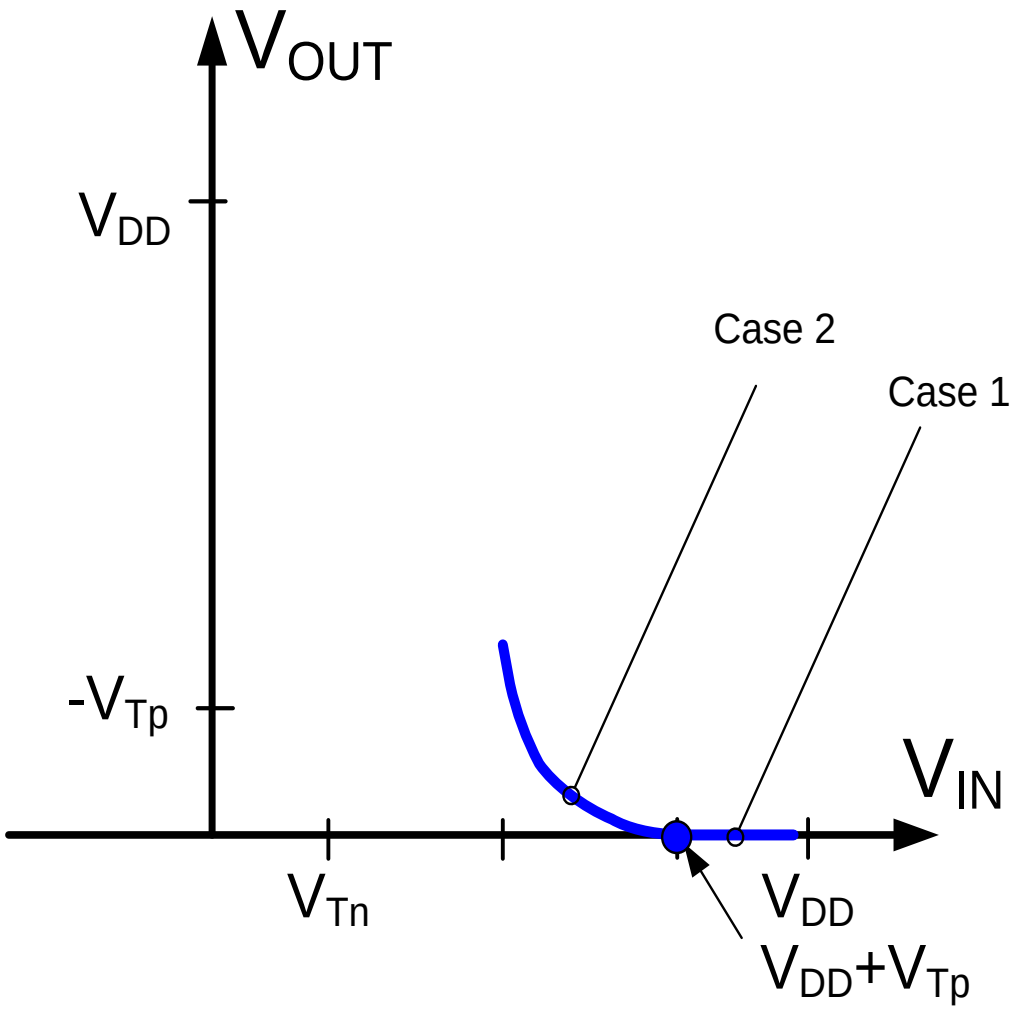
(Neglect λ effects)

Case 2 M_1 triode, M_2 sat



Transfer characteristics of the static CMOS inverter

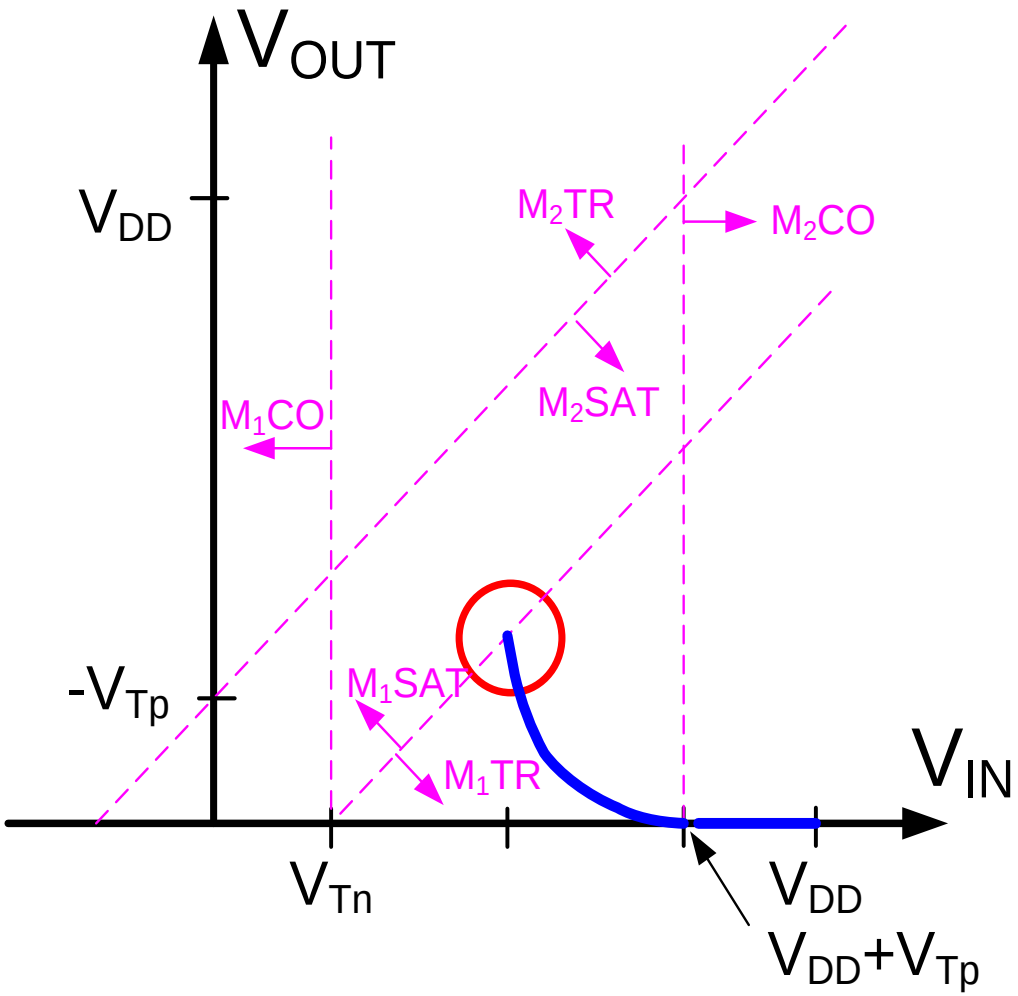
Partial solution:



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 3 M_1 sat, M_2 sat



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 3 M_1 sat, M_2 sat

$$I_{D1} = \frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2$$

$$I_{D2} = \frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp}\right)^2$$

Equating I_{D1} and $-I_{D2}$ we obtain:

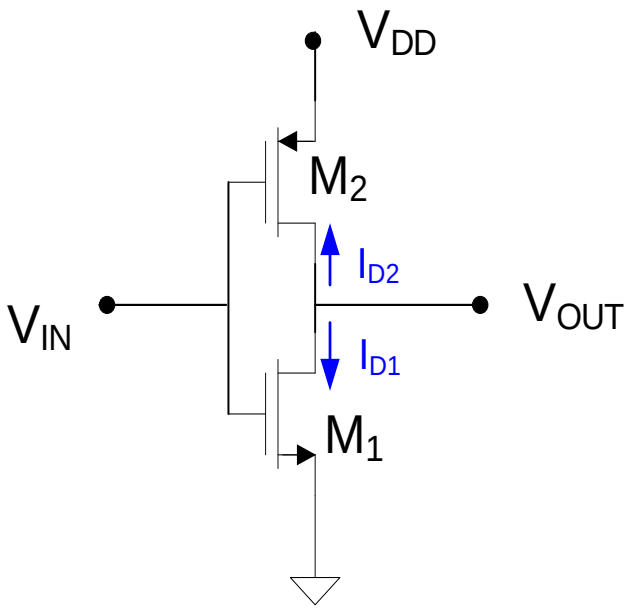
$$\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp}\right)^2 = \frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2$$

Which can be rewritten as:

$$\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}\left(V_{DD} + V_{Tp} - V_{IN}\right) = \sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}}\left(V_{IN} - V_{Tn}\right)$$

Which can be simplified to:

$$V_{IN} = \frac{\left(V_{Tn}\right)\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + \left(V_{DD} + V_{Tp}\right)\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}{\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}$$



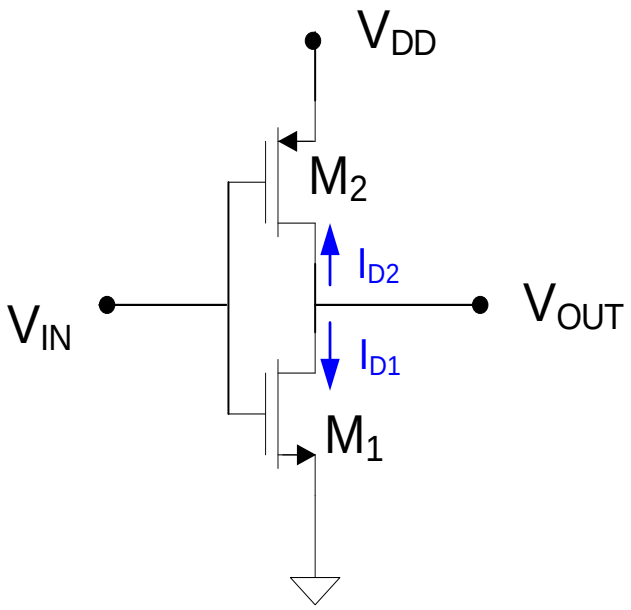
This is a vertical line

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 3 M_1 sat, M_2 sat

$$V_{IN} = \frac{(V_{Tn})\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + (V_{DD}+V_{Tp})\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}{\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}$$



Since $C_{OXn} \cong C_{OXp} = C_{OX}$ this can be simplified to:

$$V_{IN} = \frac{(V_{Tn})\sqrt{\frac{W_1}{L_1}} + (V_{DD}+V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{L_2}}}{\sqrt{\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{L_2}}}$$

valid for:

$V_{GS1} \geq V_{Tn}$ $\quad V_{DS1} \geq V_{GS1} - V_{Tn}$ $\quad V_{GS2} \leq V_{Tp}$ $\quad V_{DS2} \leq V_{GS2} - V_{T2}$

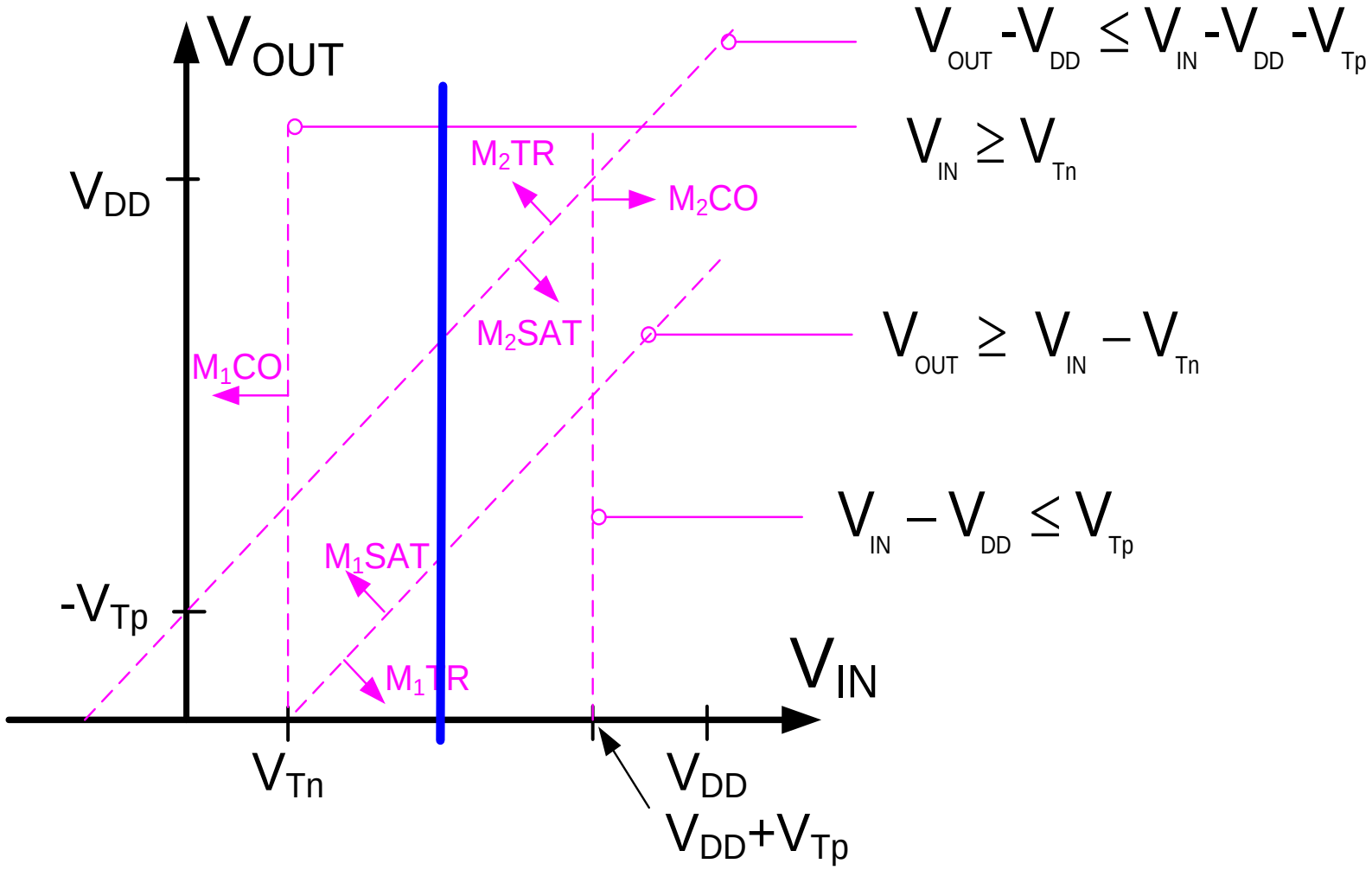
thus, valid for:

$V_{IN} \geq V_{Tn}$ $\quad V_{OUT} \geq V_{IN} - V_{Tn}$ $\quad V_{IN} - V_{DD} \leq V_{Tp}$ $\quad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

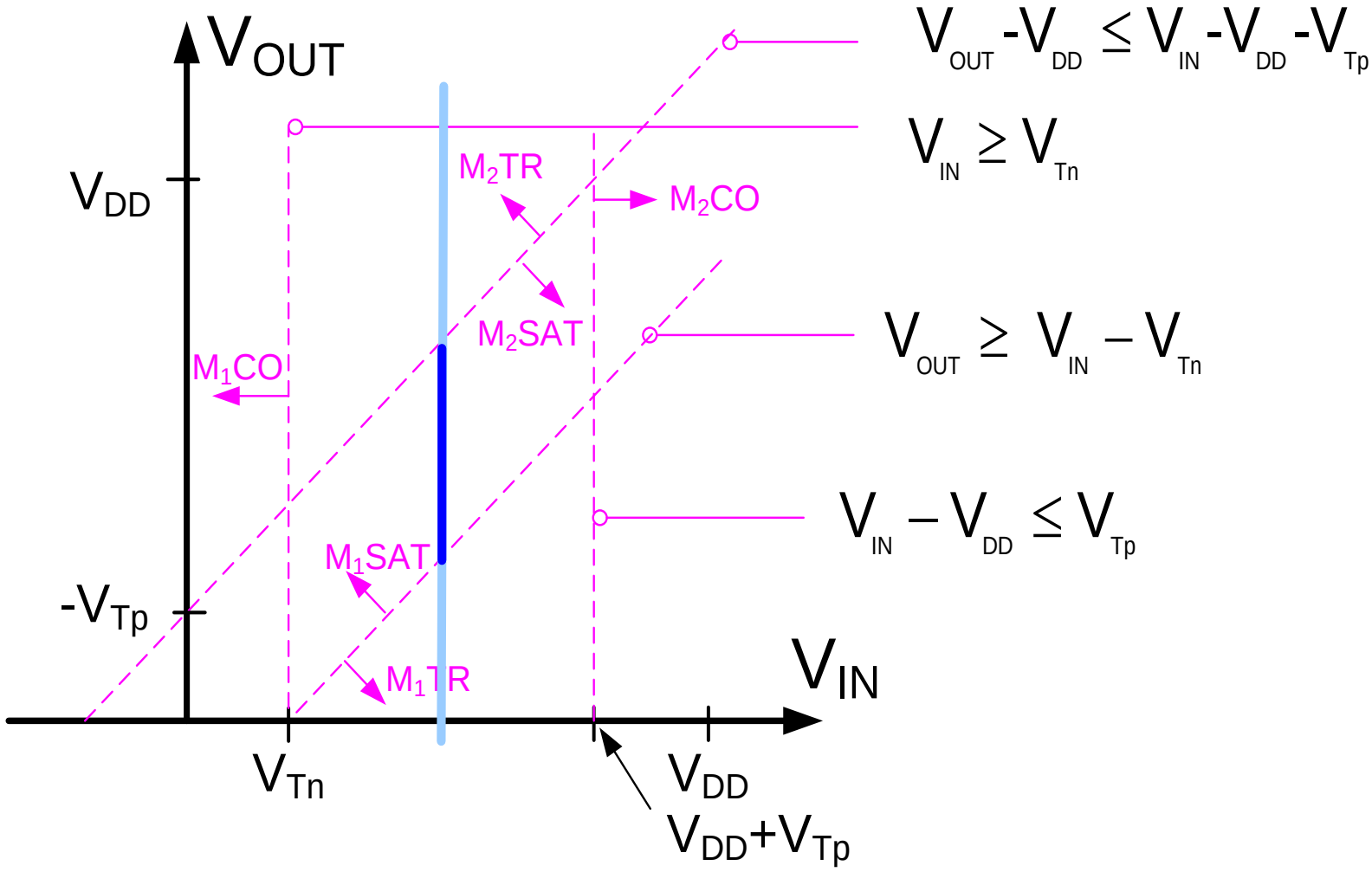
Case 3 M_1 sat, M_2 sat



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

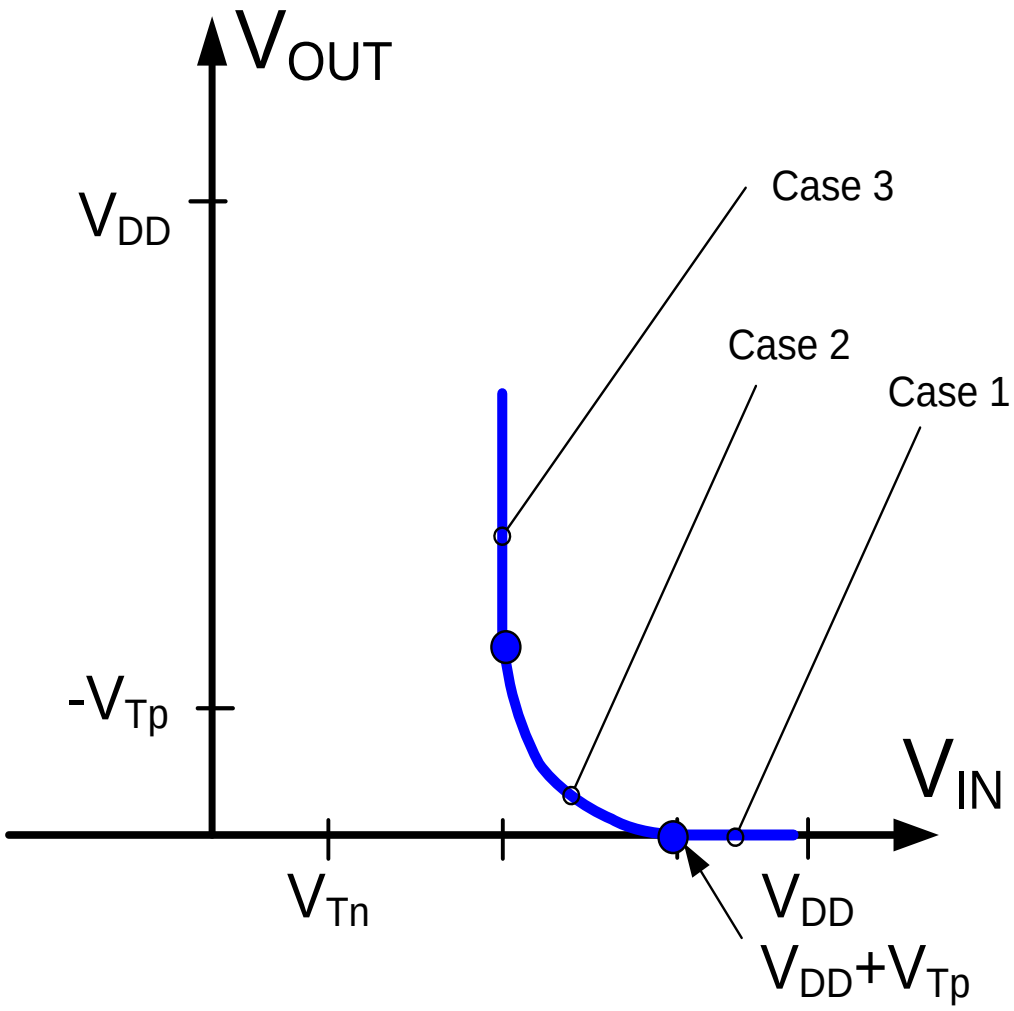
Case 3 M_1 sat, M_2 sat



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

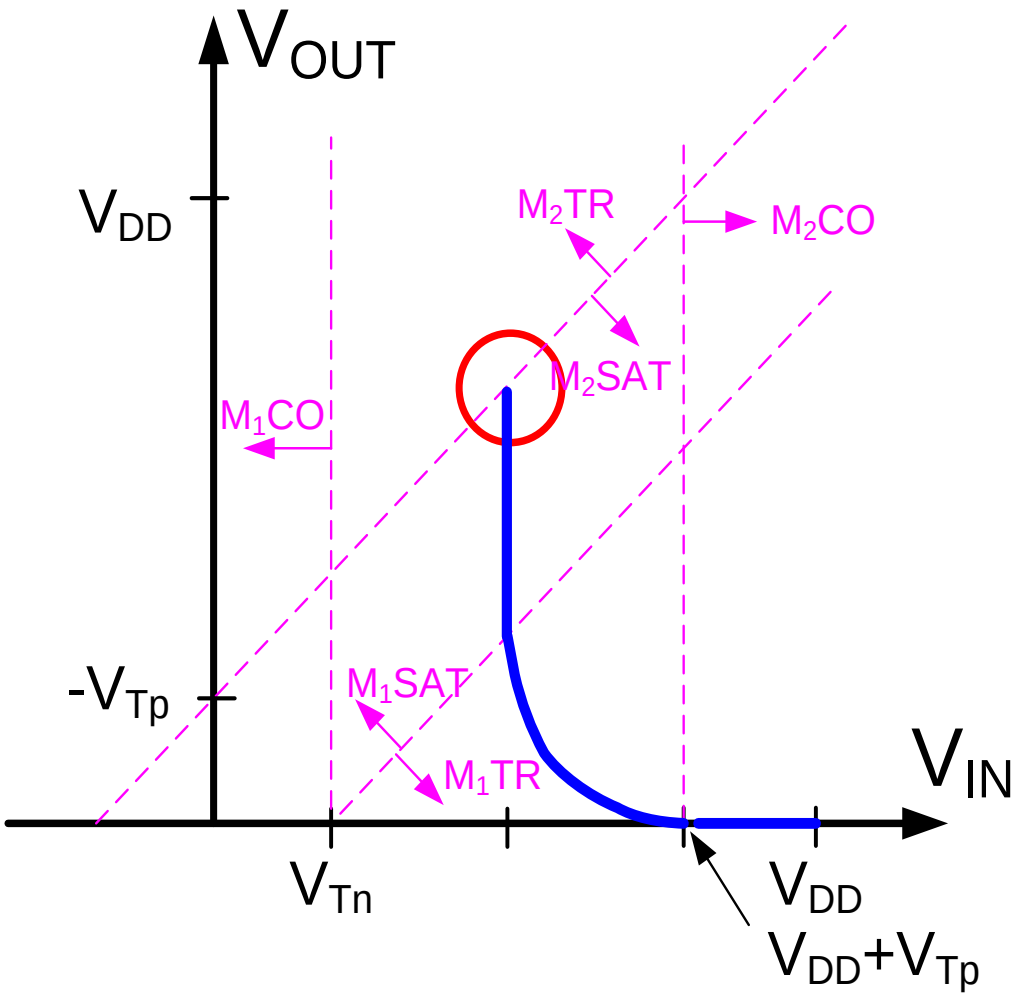
Partial solution:



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 4 M_1 sat, M_2 triode



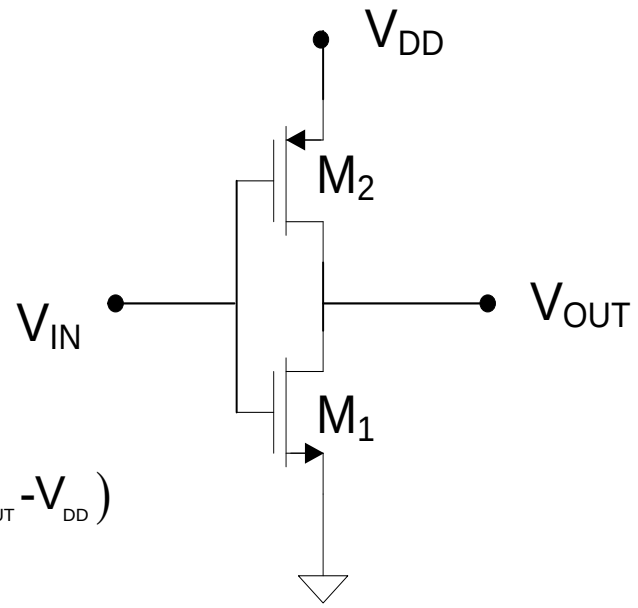
Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 4 M_1 sat, M_2 triode

$$I_{D1} = \frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2$$

$$I_{D2} = -\mu_p C_{OXp}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2}\right)\bullet\left(V_{OUT}\text{-}V_{DD}\right)$$



Equating I_{D1} and $-I_{D2}$ we obtain:

$$\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2 = \mu_p C_{OXp}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2}\right)\bullet\left(V_{OUT}\text{-}V_{DD}\right)$$

valid for:

$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} \geq V_{GS1} - V_{Tn} \qquad V_{GS2} \leq V_{Tp} \qquad V_{DS2} > V_{GS2}\text{-}V_{T2}$$

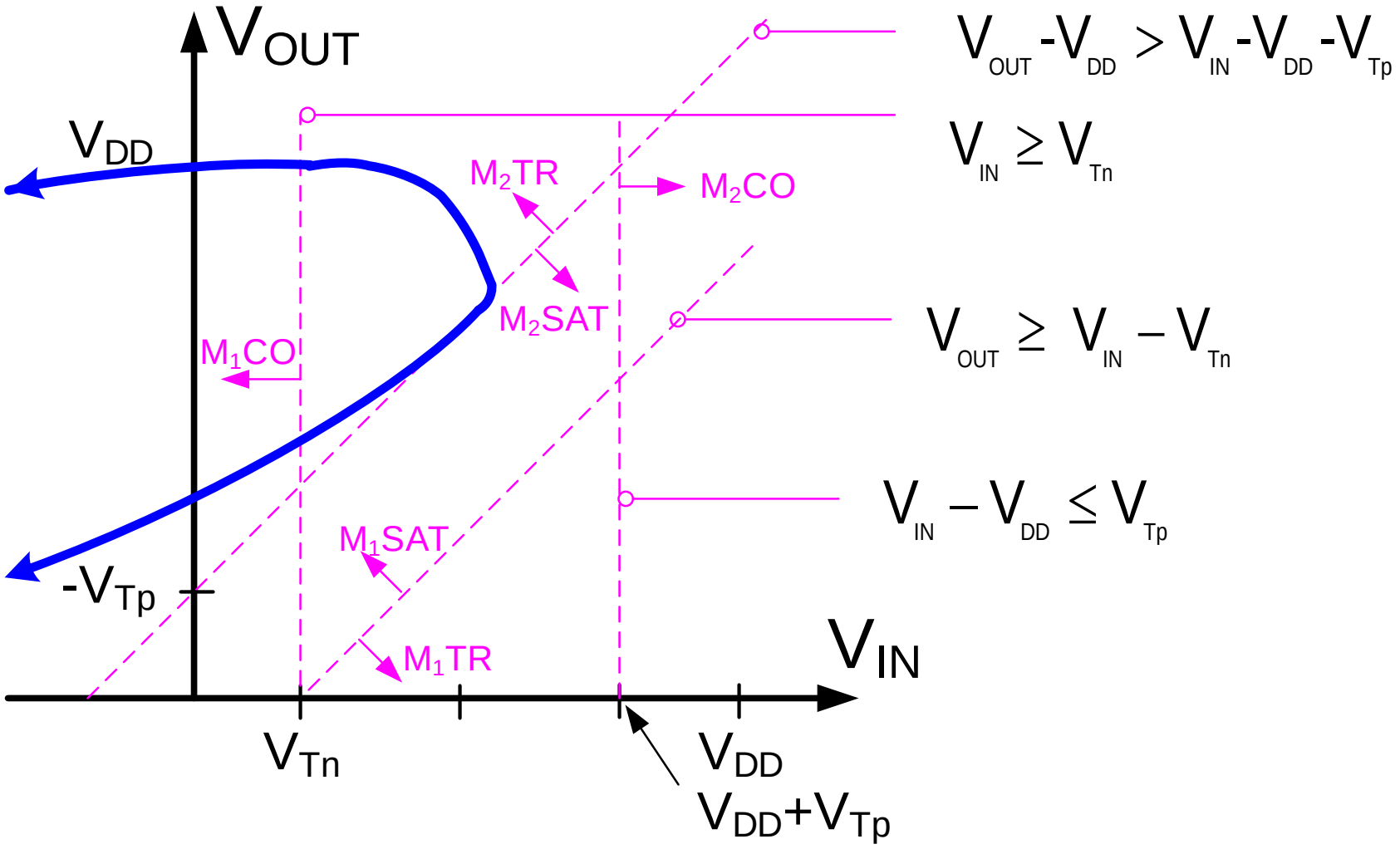
thus, valid for:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} \geq V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \leq V_{Tp} \qquad V_{OUT}\text{-}V_{DD} > V_{IN}\text{-}V_{DD}\text{-}V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

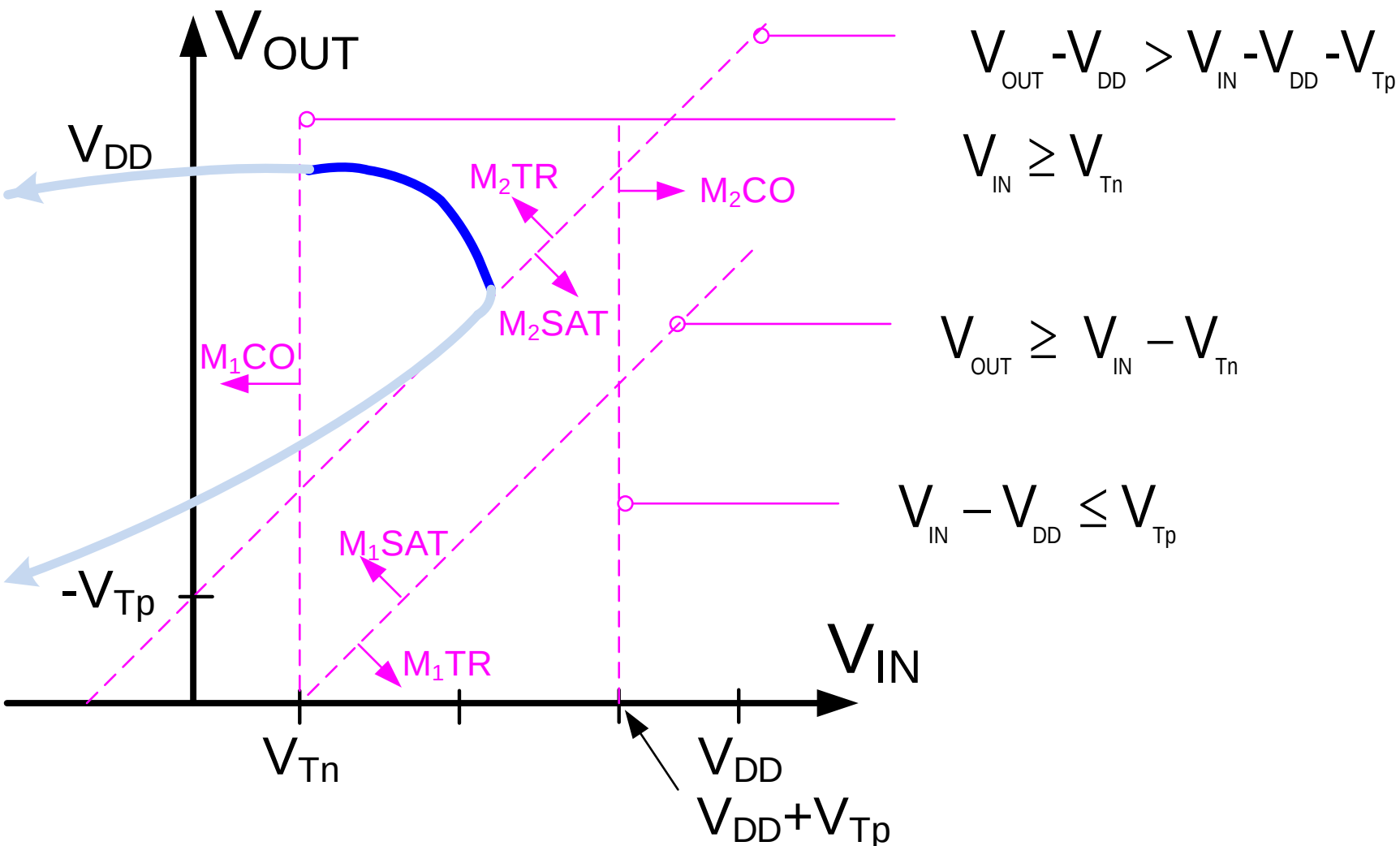
Case 4 M_1 sat, M_2 triode



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

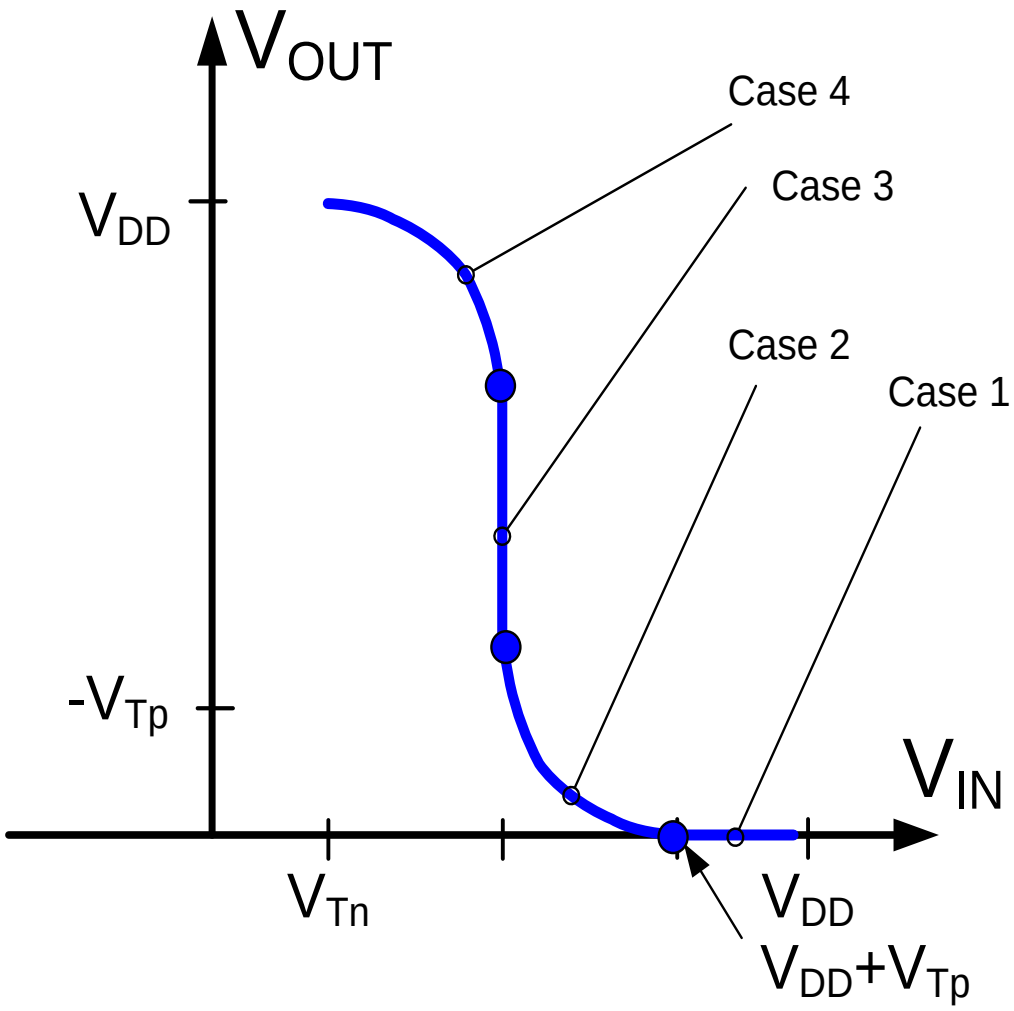
Case 4 M_1 sat, M_2 triode



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

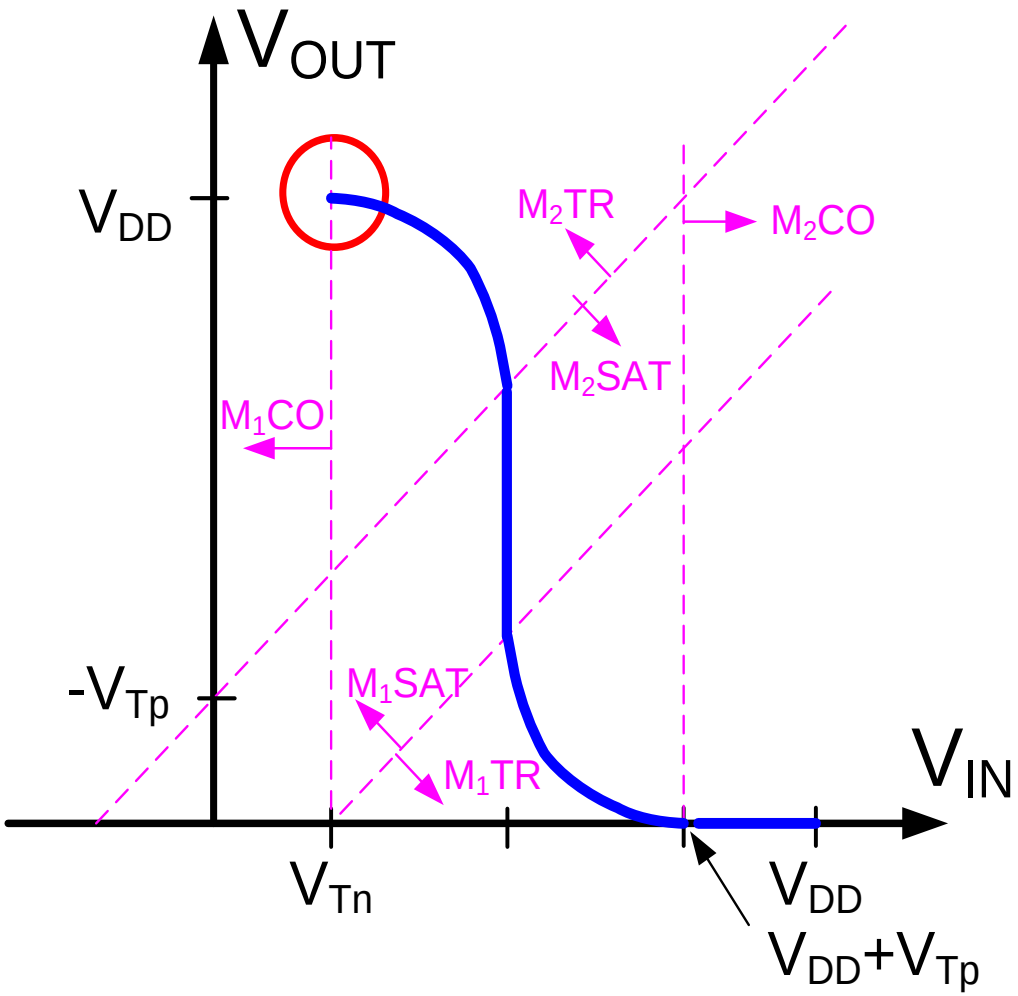
Partial solution:



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 4 M_1 cutoff, M_2 triode



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

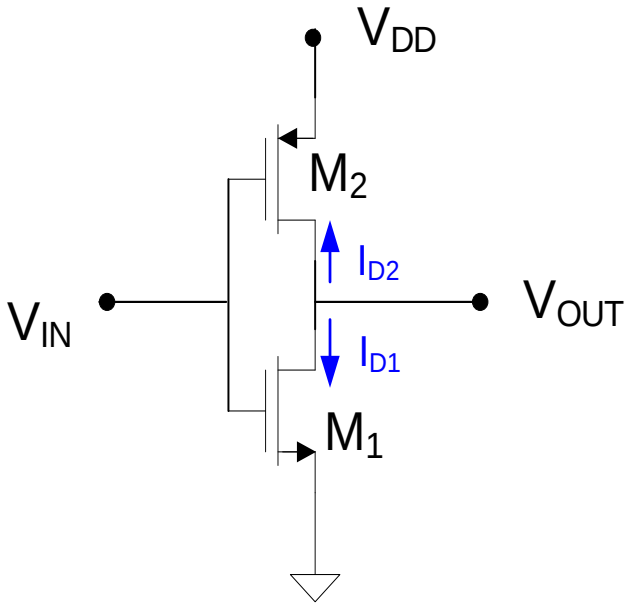
Case 5 M_1 cutoff, M_2 triode

$$I_{D1} = 0$$

$$I_{D2} = -\mu_p C_{OXp} \frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2} \right) \bullet \left(V_{OUT}\text{-}V_{DD} \right)$$

Equating I_{D1} and $-I_{D2}$ we obtain:

$$\mu_p C_{OXp} \frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2} \right) \bullet \left(V_{OUT}\text{-}V_{DD} \right) = 0$$



valid for:

$$V_{GS1} < V_{Tn} \qquad V_{GS2} \leq V_{Tp} \qquad V_{DS2} > V_{GS2} - V_{T2}$$

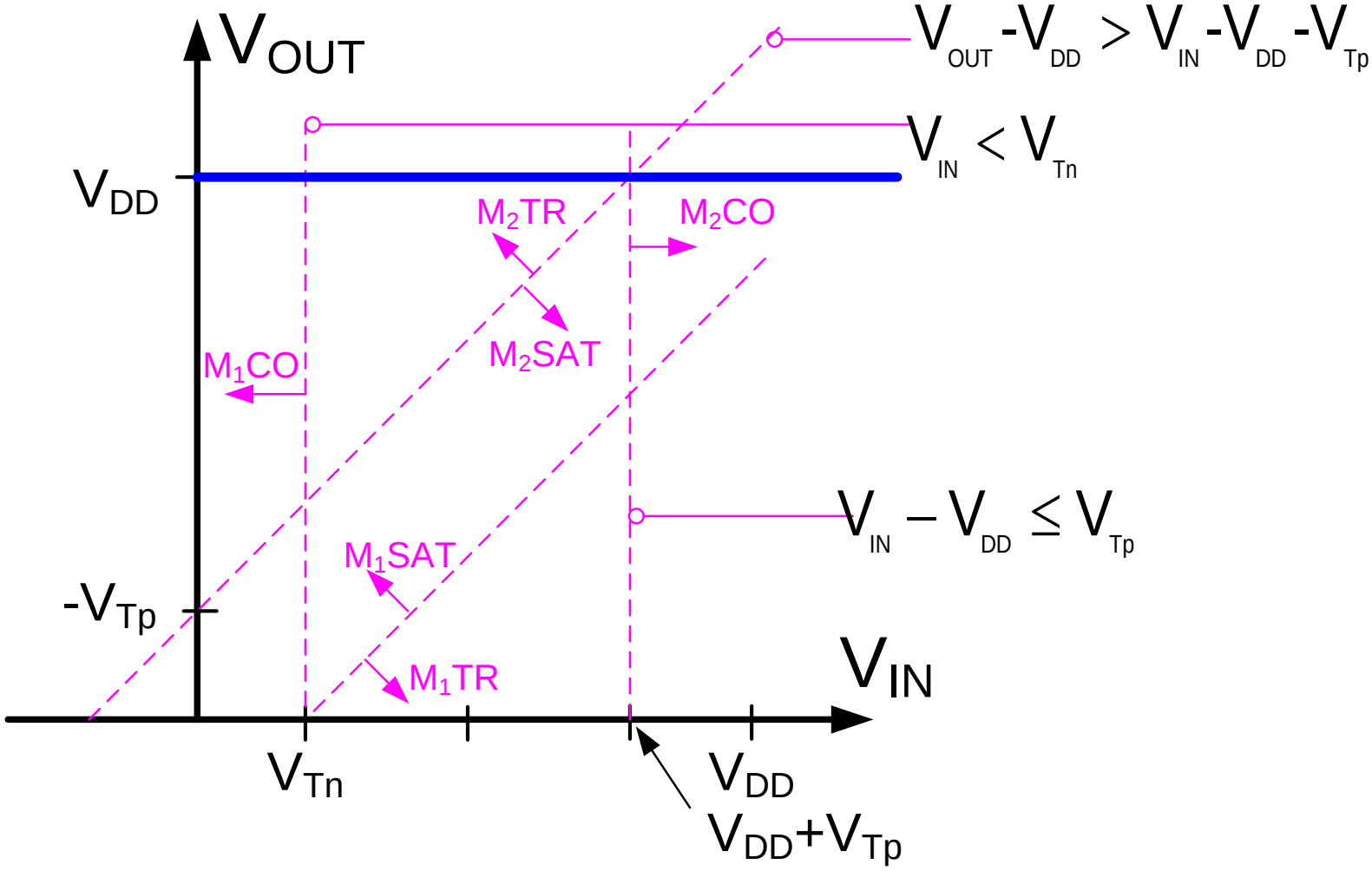
thus, valid for:

$$V_{IN} < V_{Tn} \qquad V_{IN} - V_{DD} \leq V_{Tp} \qquad V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

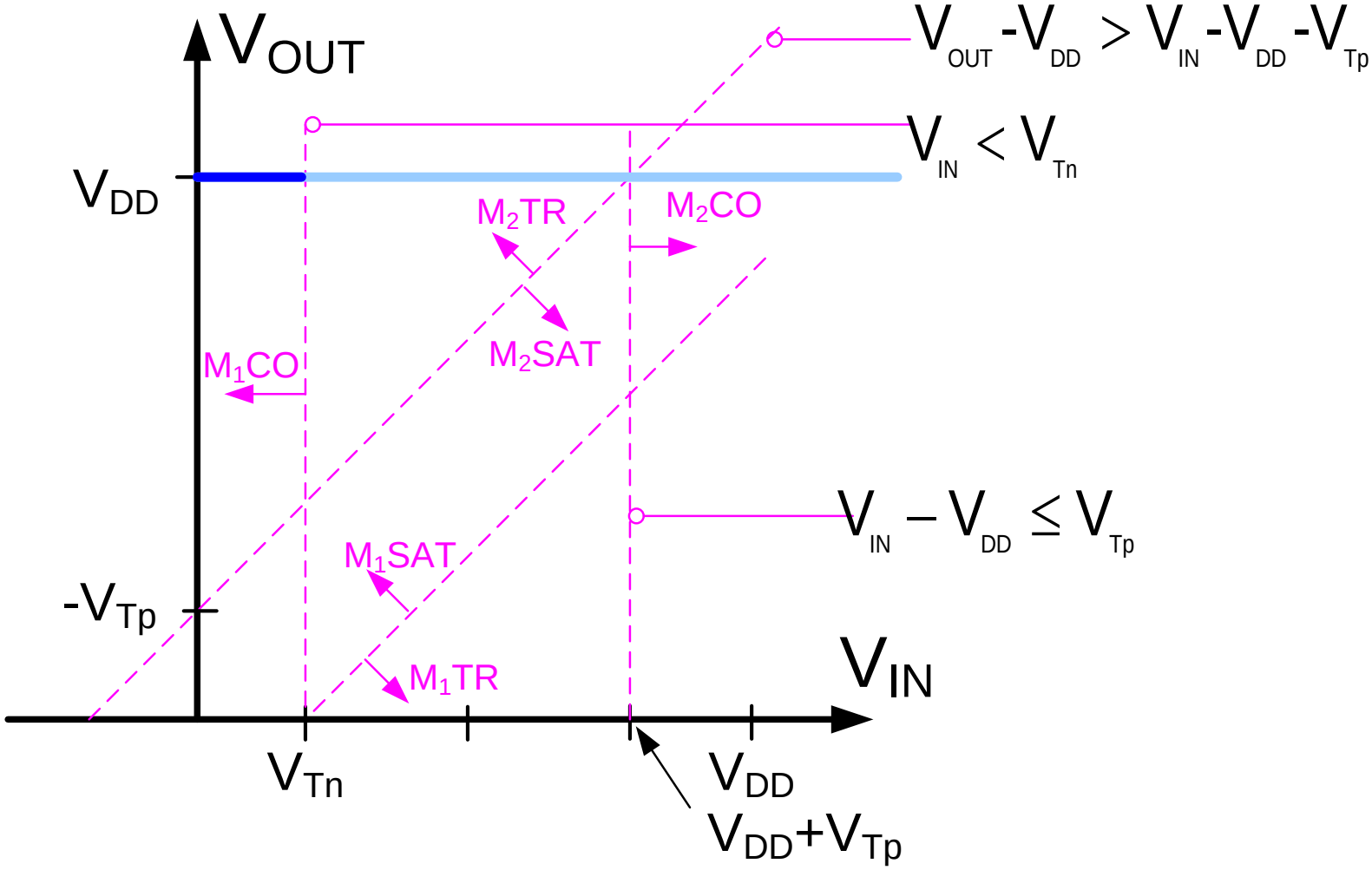
Case 5 M_1 cutoff, M_2 triode



Transfer characteristics of the static CMOS inverter

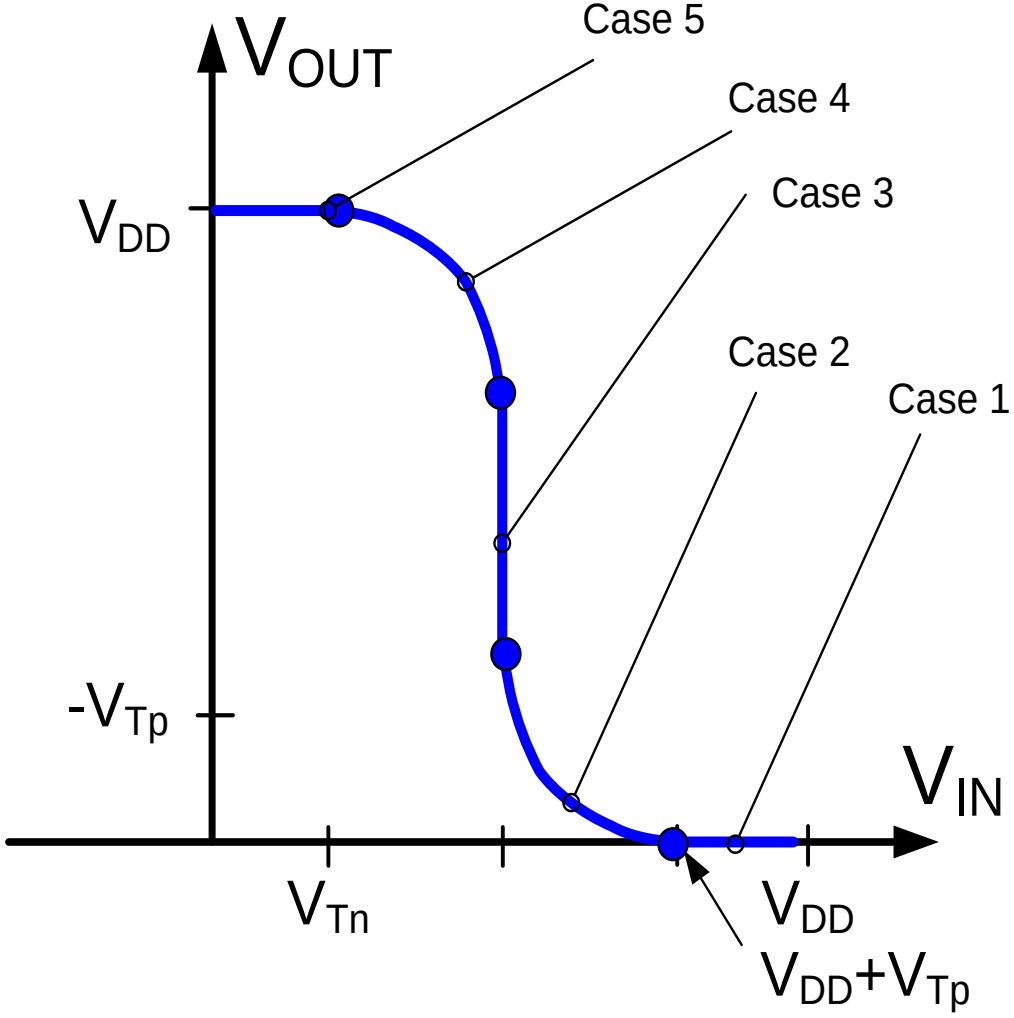
(Neglect λ effects)

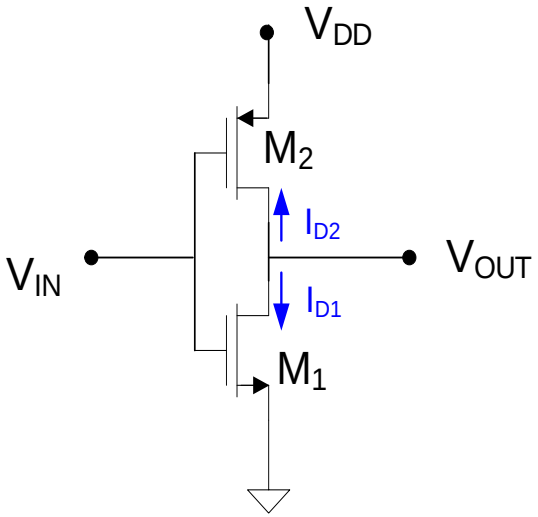
Case 5 M_1 cutoff, M_2 triode



Transfer characteristics of the static CMOS inverter

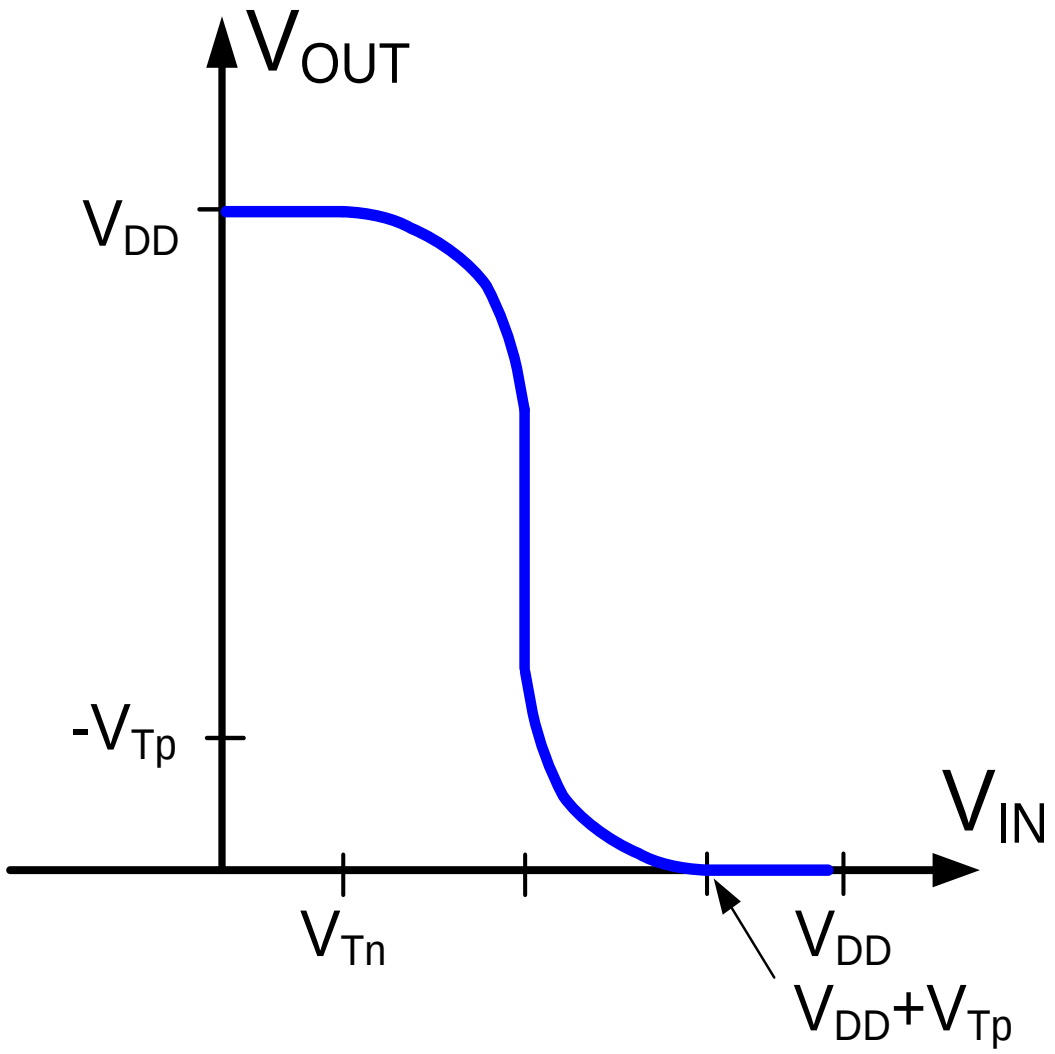
(Neglect λ effects)





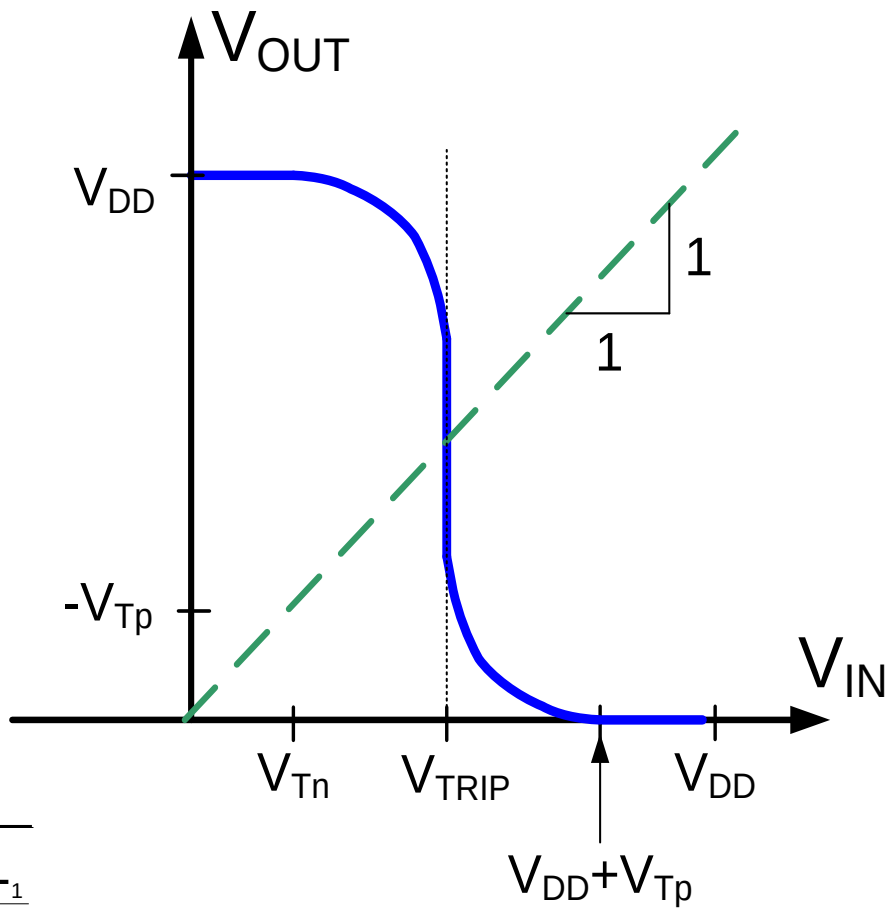
Transfer characteristics of the static CMOS inverter

(Neglect λ effects)



Transfer characteristics of the static CMOS inverter

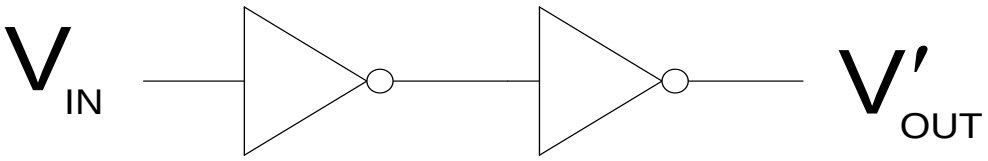
(Neglect λ effects)



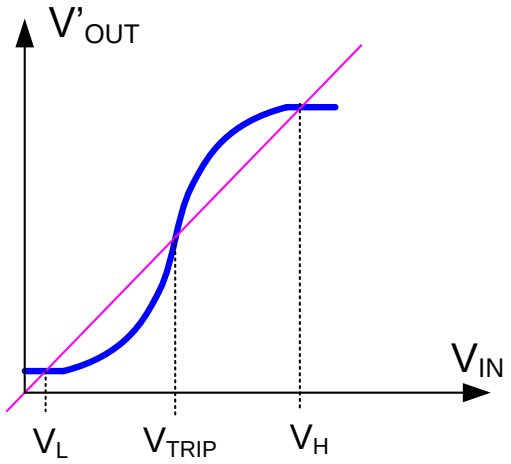
From Case 3 analysis:

$$V_{IN} = \frac{\left(V_{Tn}\right) + \left(V_{DD} + V_{Tp}\right)\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}$$

Inverter Transfer Characteristics of Inverter Pair

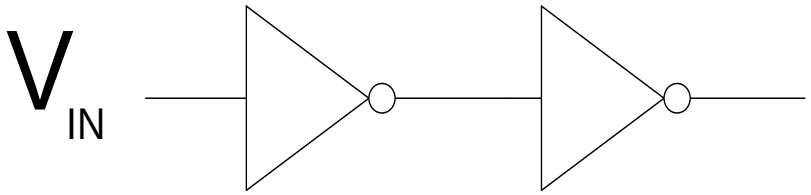


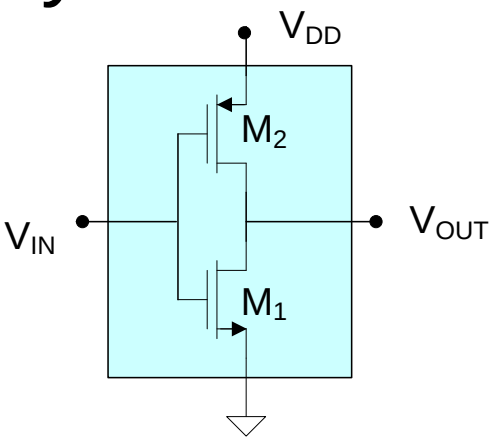
What are V_H and V_L?

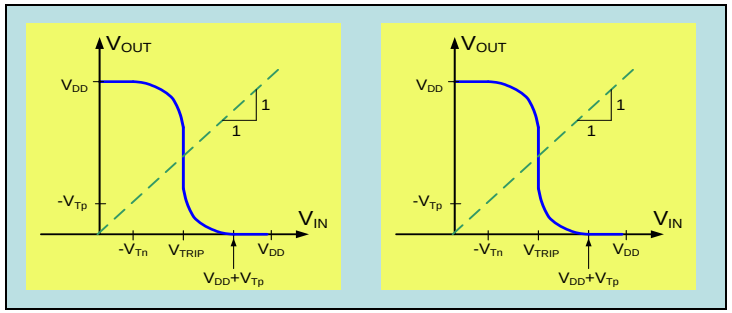


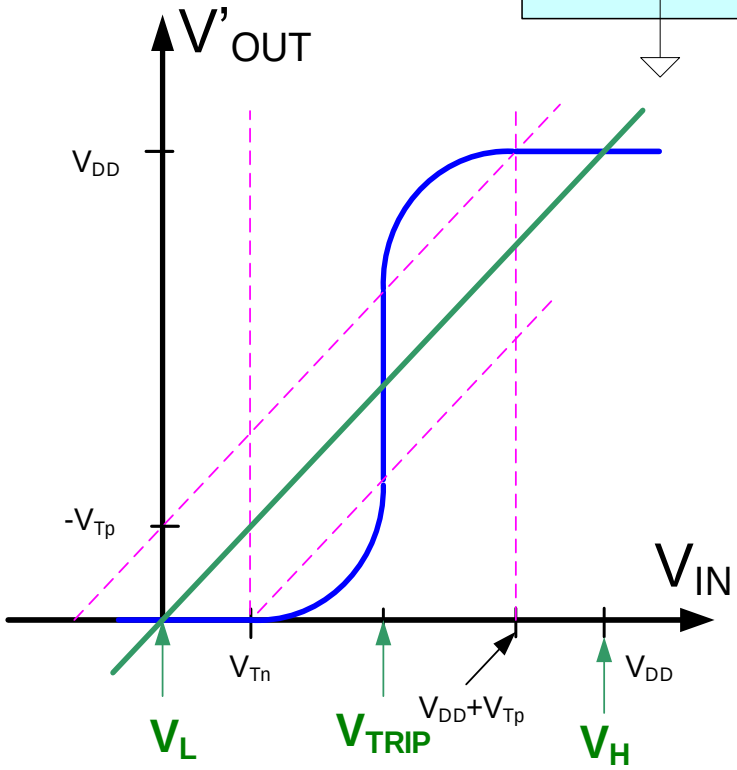
Find the points on the inverter pair transfer characteristics where V_{OUT}'=V_{IN} and the slope is less than 1

Inverter Transfer Characteristics of Inverter Pair for THIS Logic Family





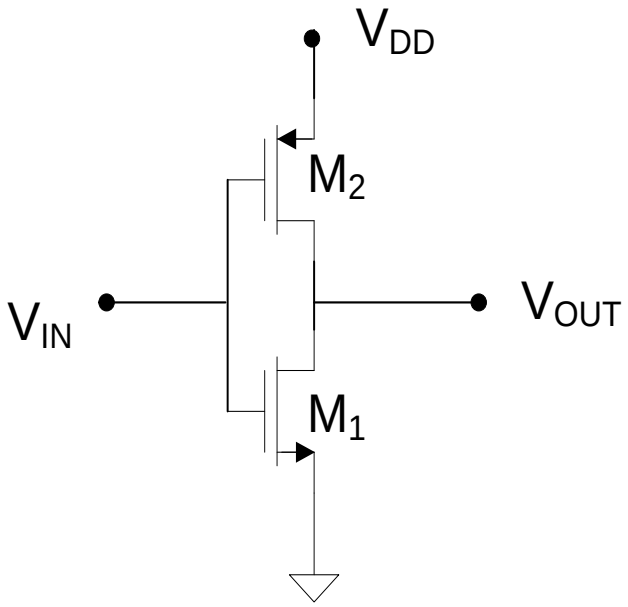




$V_H = V_{DD}$ and $V_L = 0$

Note this is independent of device sizing for THIS logic family !!

Sizing of the Basic CMOS Inverter

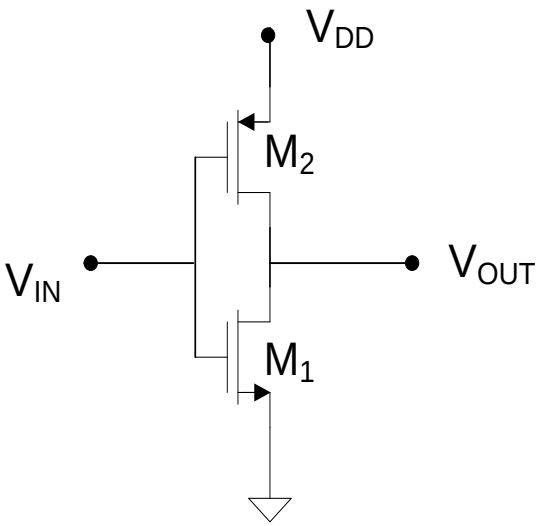


The characteristic that device sizes do not need to be used to establish V_H and V_L logic levels is a major advantage of this type of logic

How should M_1 and M_2 be sized?

How many degrees of freedom are there in the design of the inverter?

How should M_1 and M_2 be sized?



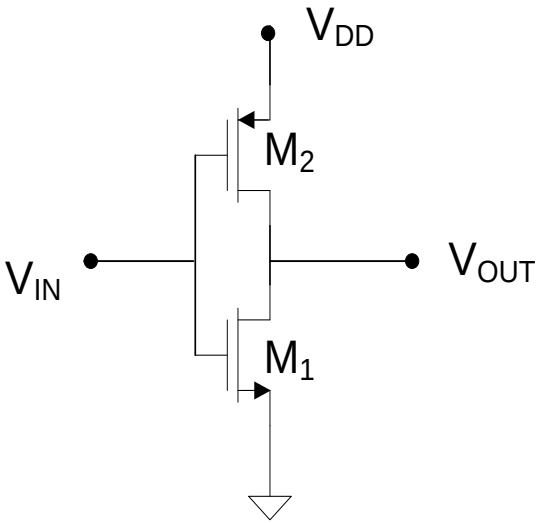
How many degrees of freedom are there in the design of the inverter?

$\{ W_1, W_2, L_1, L_2 \}$ 4 degrees of freedom

But in basic device model and in <u>most</u> performance metrics, W_1/L_1 and W_2/L_2 appear as ratios

$\{ W_1/L_1, W_2/L_2 \}$ effectively 2 degrees of freedom

How should M_1 and M_2 be sized?



$\{ W_1, W_2, L_1, L_2 \}$ 4 degrees of freedom Usually pick $L_1=L_2=L_{min}$

That leaves $\{ W_1, W_2 \}$ effectively 2 degrees of freedom

How are W_1 and W_2 chosen?

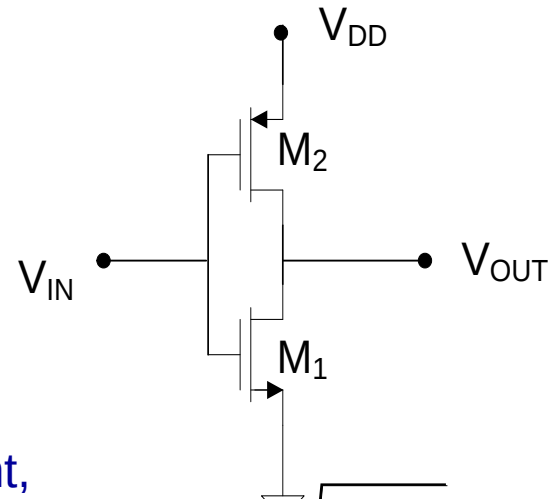
Depends upon what performance parameters are most important for a given application!

How should M_1 and M_2 be sized?

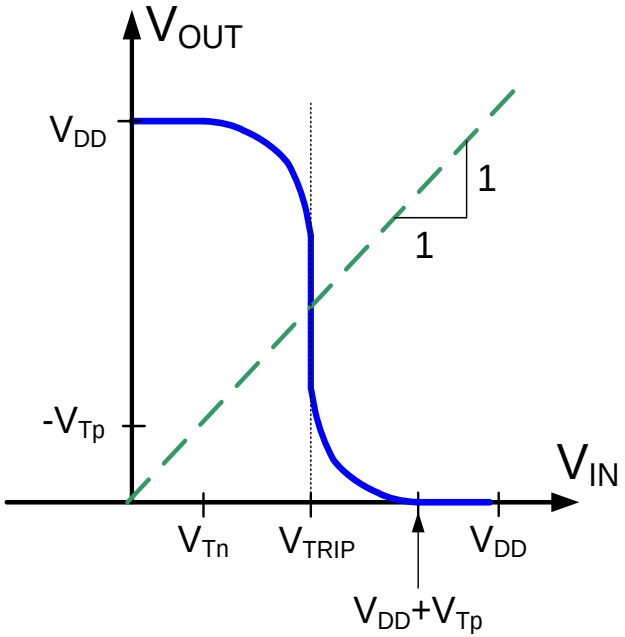
Pick $L_1=L_2=L_{min}$

<u>One</u> popular sizing strategy:

1. Pick $W_1=W_{MIN}$ to minimize area of M_1
2. Pick W_2 to set trip-point at $V_{DD}/2$



Observe Case 3 provides expression for V_{TRIP}



Thus, at the trip point,

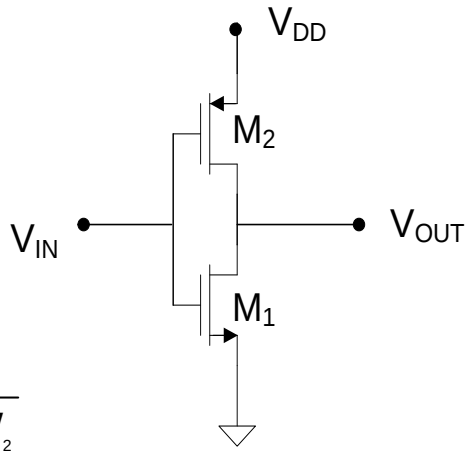
$$V_{OUT}=V_{IN}=V_{TRIP}=\frac{\left(V_{Tn}\right)+\left(V_{DD}+V_{Tp}\right)\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}}}$$

If $V_{Tn}=-V_{Tp}$

$$\frac{V_{DD}}{2}=\frac{\left(V_{Tn}\right)+\left(V_{DD}-V_{Tn}\right)\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}}}$$

How should M_1 and M_2 be sized?

Pick $L_1=L_2=L_{min}$

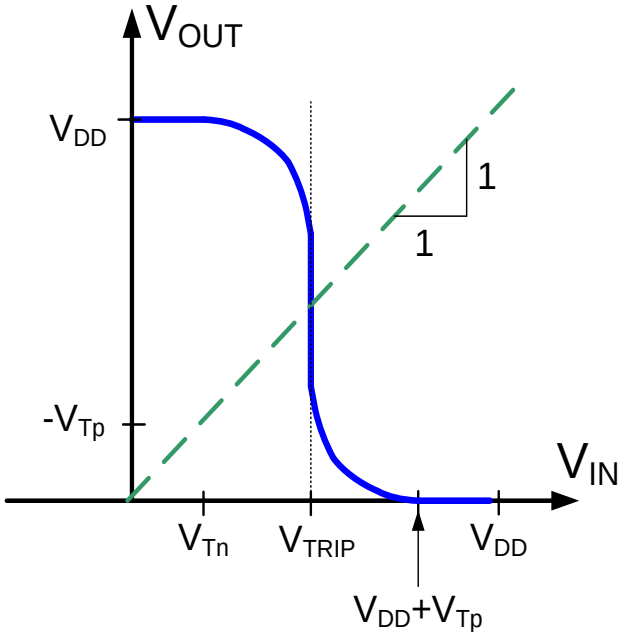


One popular sizing strategy:

1. Pick $W_1=W_{MIN}$ to minimize area of M_1
2. Pick W_2 to set trip-point at $V_{DD}/2$

Observe Case 3 provides expression for V_{TRIP}

(solution continued)



$$\frac{V_{DD}}{2}=\frac{(V_{Tn})+(V_{DD}-V_{Tn})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}}}$$

solving for $\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}}$ we obtain

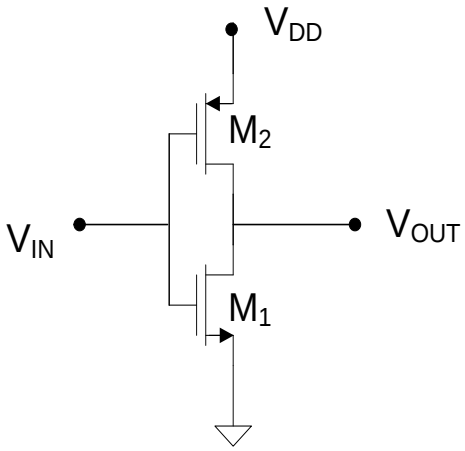
$$\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}}=\frac{V_{Tn}-\frac{V_{DD}}{2}}{-\frac{V_{DD}}{2}+V_{Tn}}=1$$

thus

$$\frac{W_2}{W_1}=\frac{\mu_n}{\mu_p} \Rightarrow W_2=\frac{\mu_n}{\mu_p}W_{MIN}\simeq 3W_{MIN}$$

How should M_1 and M_2 be sized?

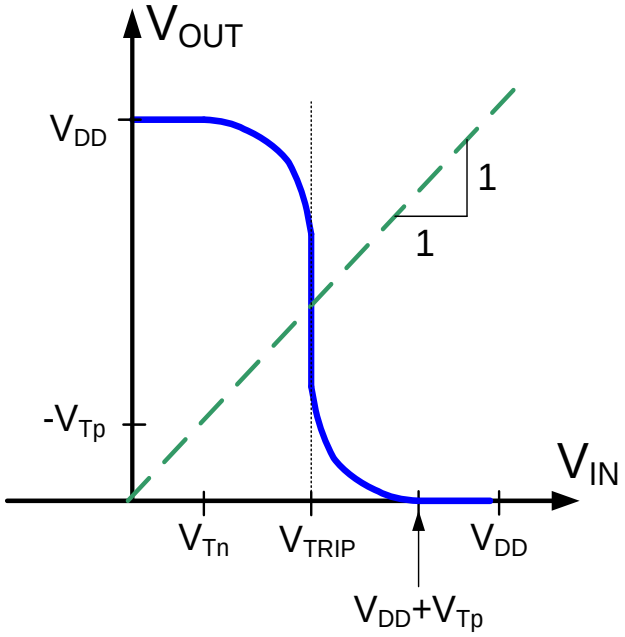
Pick $L_1=L_2=L_{min}$



<u>One</u> popular sizing strategy:

1. Pick $W_1=W_{MIN}$ to minimize area of M_1
2. Pick W_2 to set trip-point at $V_{DD}/2$

Observe Case 3 provides expression for V_{TRIP}



Summary: $V_{TRIP} = \frac{V_{DD}}{2}$ sizing strategy

$L_1=L_2=L_{min}$

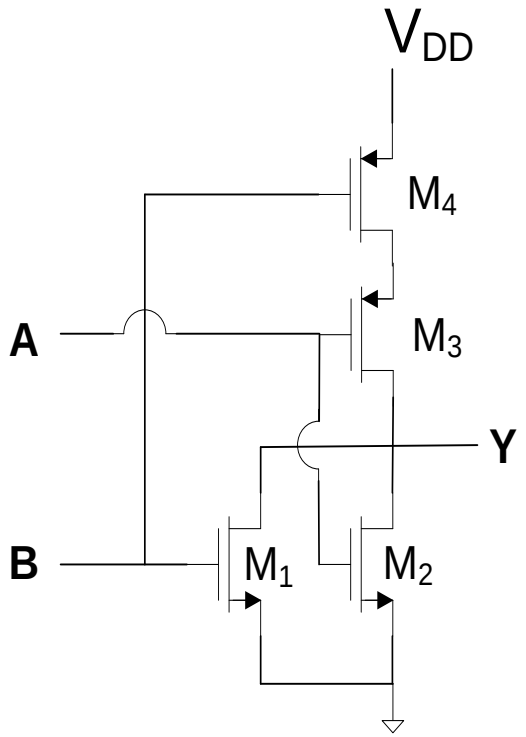
$W_1=W_{MIN}$

$W_2 = \frac{\mu_n}{\mu_p} W_{MIN} \simeq 3W_{MIN}$

(dependent upon assumption $V_{Tp}= -V_{Tn}$)

Other sizing strategies will be discussed later !

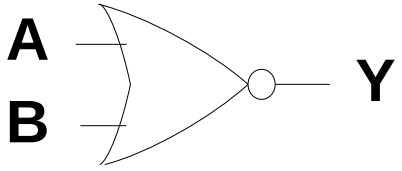
Extension of Basic CMOS Inverter to Multiple-Input Gates



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table

Performs as a 2-input NOR Gate

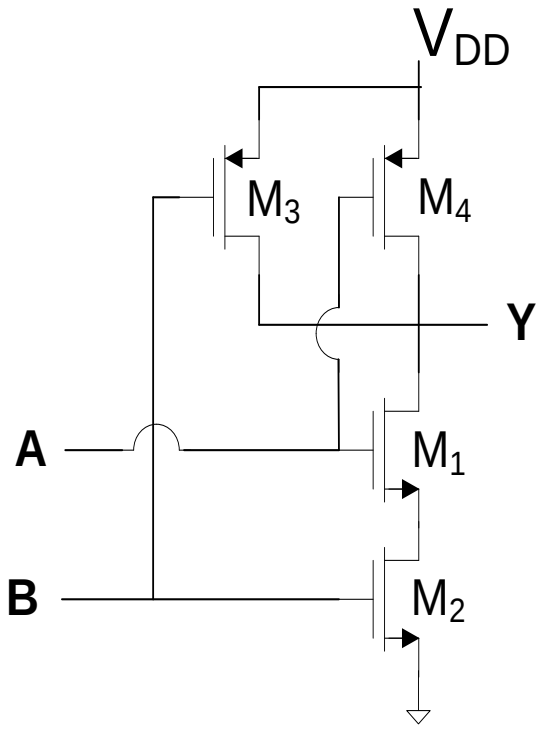


Can be easily extended to an n-input NOR Gate

$V_H=V_{DD}$ and $V_L=0$ (inherited from inverter analysis)

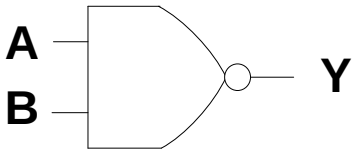
analysis not shown here but straightforward and consistent with claim that performance of gates in logic family determined by those of basic inverter

Extension of Basic CMOS Inverter to Multiple-Input Gates



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table

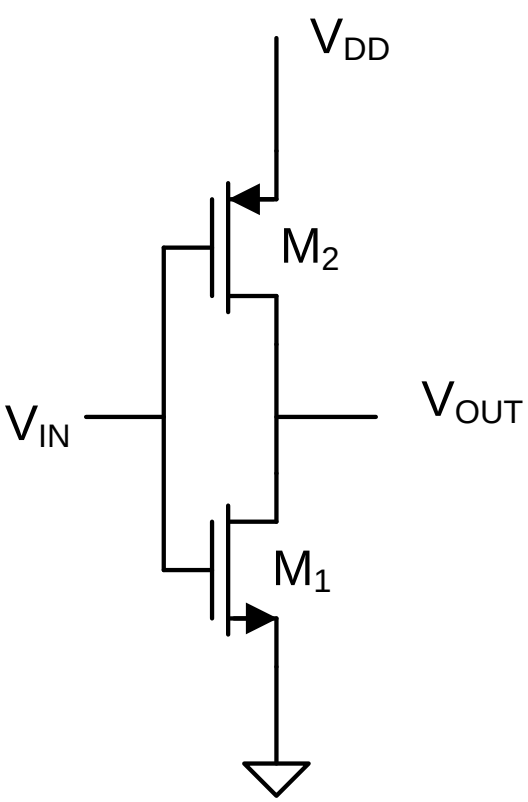


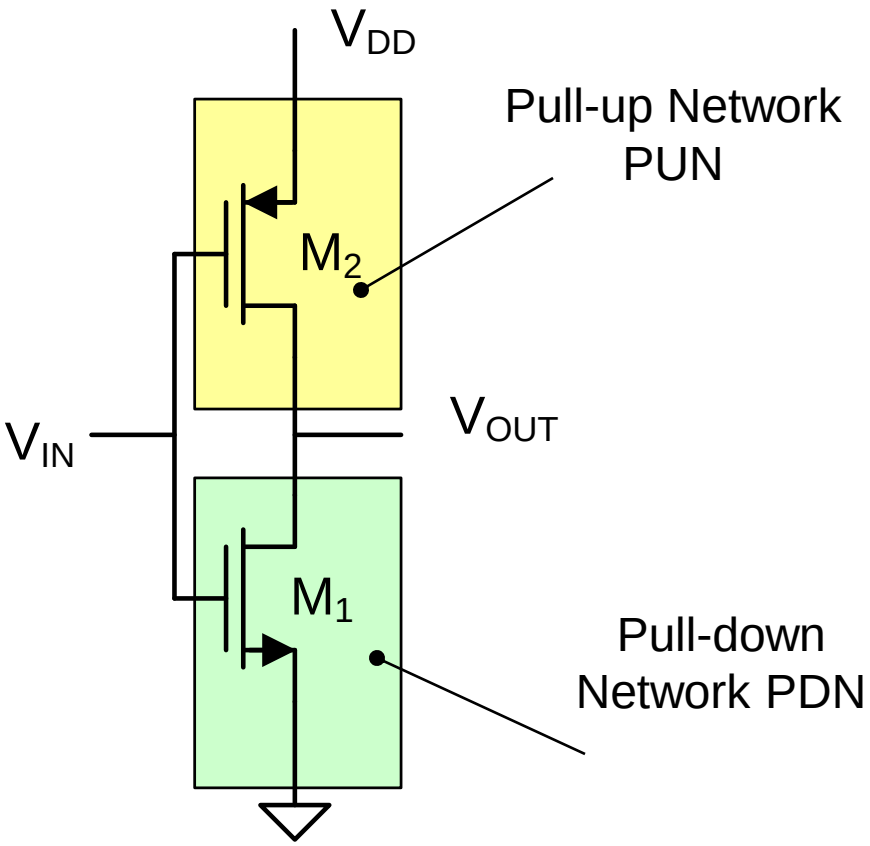
Performs as a 2-input NAND Gate

Can be easily extended to an n-input NAND Gate

$V_H=V_{DD}$ and $V_L=0$ (inherited from inverter analysis)

Static CMOS Logic Family

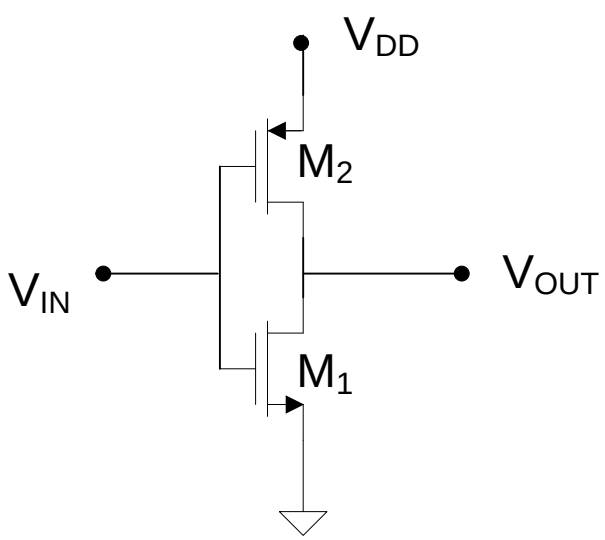


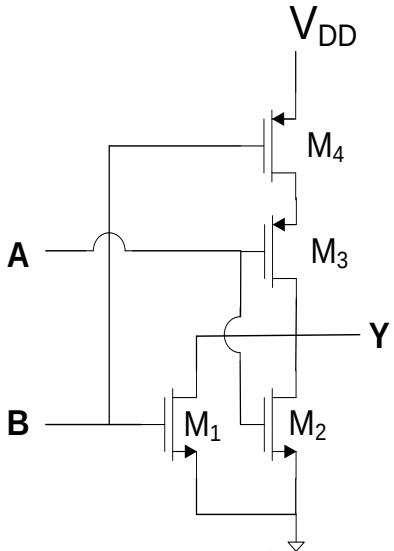


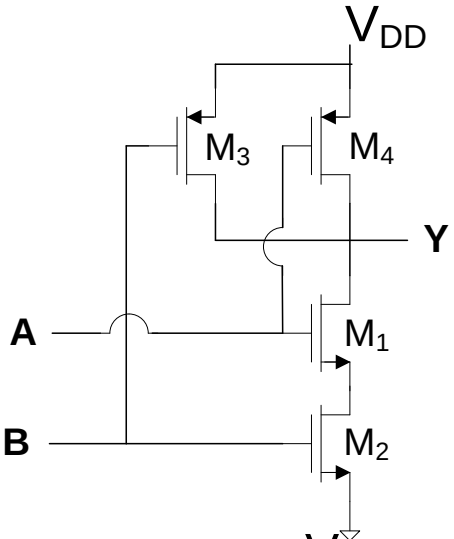
Observe PUN is p-channel, PDN is n-channel

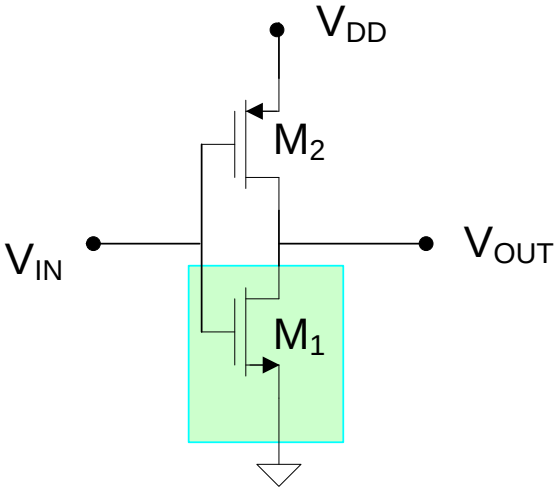
$V_H=V_{DD}$ and $V_L=0$ (inherited from inverter analysis)

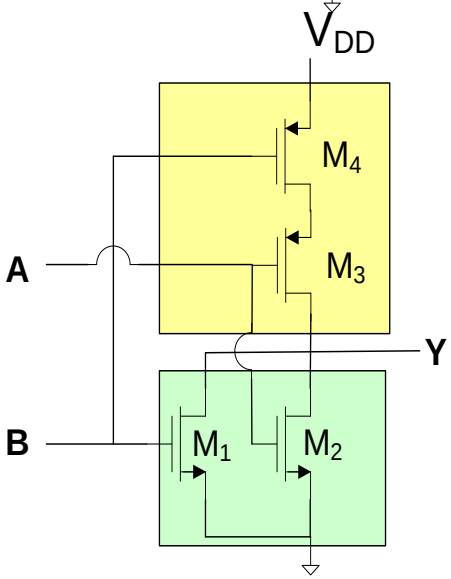
Static CMOS Logic Family

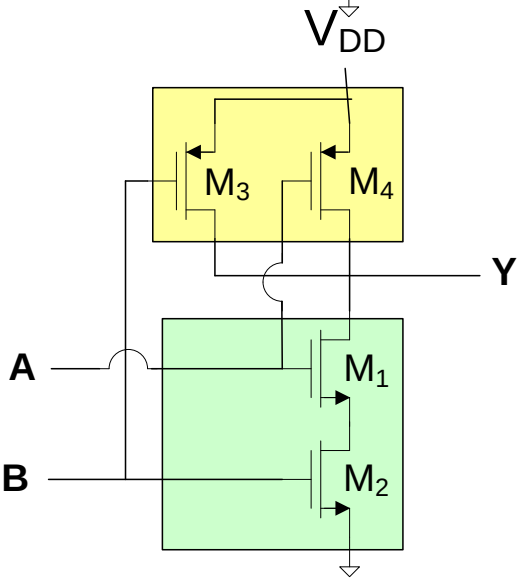












n-channel PDN and p-channel PUN

$V_H=V_{DD}$, $V_L=0V$ (same as for inverter!)

Stay Safe and Stay Healthy !

End of Lecture 37